EMaper: Cross-level Electromigration Aware Placement and Routing EDA Workflow for Interconnects Hotspot Prediction and Mitigation

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***Abstract*—Electromigration (EM) has emerged as a critical reliability concern in advanced technology nodes. Yet the industry-standard Black's equation lacks generality because its fitted parameters depend strongly on interconnect geometry and can only applied for single segment. In addition, conventional post-layout "analyze-then-fix" verification is reactive and ill-suited to varying mission profiles with stringent EM targets. In this work, we propose EMaper, a cross-level EM-aware optimization framework that couples physics-grounded modeling with early placement and routing. EMaper introduces: (1) a physics-informed EM compact model and thermal simulator, enabling accurate EM estimation across varying geometries and conditions and full-chip thermal analysis; (2) a physically predictive placement and routing framework integrated with physical models. (3) A cross-level framework—spanning from the atomic scale to the physical model to EDA flow—enabling in-design violation prediction and mitigation across varying application scenarios. Experimental results on the ISPD2018 benchmarks demonstrate that EMaper eliminates 92.1% to 100% of EM violations across a variety of operating conditions, with only 4.49% to 16.3% overhead in wirelength and via count. Furthermore, in thermally benign scenarios (e.g., 300 K), EMaper naturally incurs zero overhead, reflecting its self-adaptive optimization capability. These results highlight EMaper's potential as a practical and scalable solution for EM-aware physical design in modern VLSI flows.**

***Index Terms*—electromigration, cross-level co-optimization, thermal, placement, routing**

I. Introduction

With continued IC scaling and rising current densities, electromigration (EM) has become a critical reliability challenge, making in-flow EM assessment essential. Many physical models have been explored [1-5], yet industry EDA still favors Black's Equation for its simplicity and easy calibration[6]:

$$mTTF = Aj^n \exp\left(\frac{E_a}{kT}\right) \quad (1)$$

where j is the current density, n the current exponent, k the Boltzmann's constant, T the temperature (K) and E_a the EM activation energy. The empirical prefactor A depends on material and geometry and varies across technology nodes and scales; thus, EM characterization at different geometries requires extracting a case-specific A via standard EM tests [7], which is time-consuming and resource-intensive. A geometry-aware compact model is therefore needed to complement Black's Equation for design-level EM estimation. Moreover, Black's equation implies strong temperature sensitivity [8] —even a 10 K variation can reduce mean time to failure (mTTF) by nearly 50%—so EDA EM models require accurate sign-off temperature. In practice, EM analyses commonly assume a uniform die temperature and ignore lateral variations, leading to overly conservative design margins [9]. A BEOL-tailored thermal solver is therefore needed. On the other hand, traditional EM evaluation methods typically follow an "analyze-then-fix" approach: violations are found after physical verification and circuit simulation, leading to multiple iterations, especially at advanced nodes and under demanding mission profiles. For example, applications such as electrical vehicles [9] and aerospace systems [10] exhibit large temperature swings and stringent EM requirements. Yet mainstream digital P&R tools either overlook these concerns or lack low-level physical grounding [11, 12] , because incorporating real mission profiles [13] during early placement and routing is inherently challenging. Since strict EM analysis/optimization typically relies on the EM techfile available post-layout, it is crucial to quantify actual physical impacts on EM reliability and integrate corresponding optimization into placement and routing.

To overcome the limitations of post-layout EM verification, we present EMaper, an EM-aware placement-and-routing (P&R) framework for in-design prediction and mitigation of interconnect hotspots. Our contributions are threefold:

- **Physics-informed EM Compact Model & Thermal Simulator**: (a) An atomistic, geometry-aware EM model that generalizes across geometries and conditions, robust under scarce data. (b) A GPU accelerated full-chip thermal simulator based on 3D thermal resistor network.
- **Physical Predictor incorporated Placer and Router:** (a) A power aware placement strategy enlightened by steady state heat diffusion equation; (b) Global routing integrated with the thermal simulator and EM compact model, using an EM-techfile–derived cost scheme and a Dijkstra-based routing algorithm.
- **A Cross-Level EM Aware Optimization Work Flow:** A cross-level framework—spanning from the atomic scale to the physical design level and the EDA flow—enabling in-design violation prediction and mitigation.

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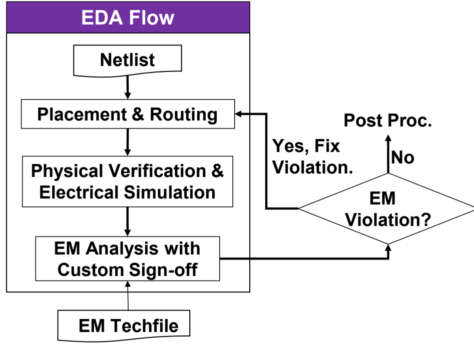


Fig. 1. Tradition EDA workflow for EM analysis and EM violation repair.

II. Background

Electromigration (EM) is the electron-momentum–driven transport of metal atoms under high current stress; the resulting voids and hillocks raise resistance, degrade signal integrity, and can cause opens. With rising power density and design complexity, EM reliability is a key physical-design concern—especially for PDNs and long global interconnects. Fig. 1 outlines the standard sign-off/repair flow: after placement and routing, DRC/LVS and PEX are performed; interconnect currents are then evaluated from the extracted netlist at the sign-off temperature. For each metal layer, the average DC current of every wire segment must be below the EM limit $I_{EM,limit}$ under application-specific conditions EOL_{app} (End of line), T (Temperature) and CDF_{app} (cumulative distribution function for failure rate) [14]. The $I_{EM,limit}$ at T_{EM} is derived from the reference conditions defined in EM techfile library using adjustment factors based on Black's Equation[6]. Segments exceeding $I_{EM,limit}$ are flagged as EM hotspots; they are fixed by re-placement and/or re-routing, with re-analysis iterated until all hotspots are cleared.

III. Method

Fig. 2 presents the EMaper workflow, integrating atomic-level modeling with EDA-level EM-aware co-optimization. This section details: (i) atomic-level calculations, (ii) compact-model–based EM techfile extraction, (iii) multiscale thermal simulation, and (iv) EM-aware placement and routing.

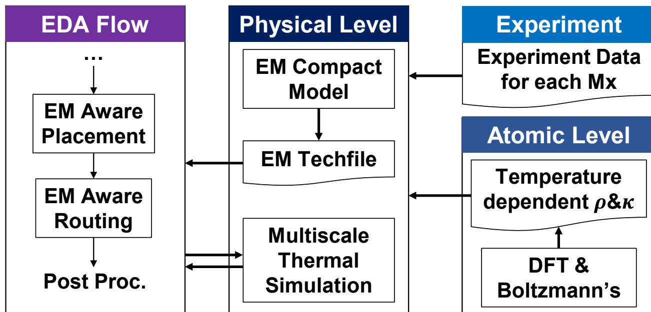


Fig. 2. EMaper Overall flow: atomic-physical-EDA cross-level EM-aware co-optimization.

A. Atomic-level Simulation for Temperature Dependent Microscope Parameters

To ensure self-consistency, we couple Boltzmann transport with first-principle calculation to extract temperature dependent parameters of interconnect metal [15].

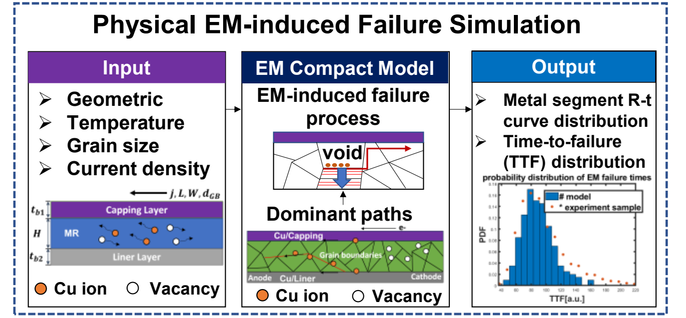


Fig. 3. EM-induced failure simulation based on EM compact model.

The conductivity σ and thermal conductivity κ_e can be defined as [16] :

$$\sigma(\mu,T) = L^{(0)}(\mu,T), \quad \kappa_e(\mu,T) = \frac{1}{q^2T}\left[\frac{\left(L^{(1)}\right)^2}{L^{(0)}} - L^{(2)}\right] \tag{2}$$

Where $L^{(\alpha)}(\mu,T)$ are generalized transport coefficients determined by electron group velocity. The relaxation time τ is given within considering electron phonon scattering theory:

$$\tau = \hbar\left(\mathrm{Im}\Sigma_{n,k}\right)^{-1} \tag{3}$$

Where $\Sigma_{n,k}$ is the electron self-energy considering electron phonon scattering matrix $g(k,q)$:

$$\Sigma_{n,k} = \sum_{qv,m} w_q\left|g_{mn,v}(k,q)\right|^2 \Big[\frac{n(\omega_{qv}) + f(\epsilon_{m\,k+q})}{\epsilon_{nk} - \epsilon_{m\,k+q} + \omega_{qv} - i0^+} + \frac{n(\omega_{qv}) + 1 - f(\epsilon_{m\,k+q})}{\epsilon_{nk} - \epsilon_{m\,k+q} - \omega_{qv} - i0^+}\Big] \tag{4}$$

B. EM techfile Extraction Based on Compact Model

Fig. 3 illustrates the EM-induced failure simulation using the compact model [17]. For each metal segment, geometry (length, width, grain size), temperature, and current density are provided as inputs. The model resolves the EM failure process—nucleation, void formation, and growth [18] —and accounts for dominant atomic-migration pathways (cap/metal interface, metal/liner interface, grain boundaries) [19]. The compact model is used to generate the EM techfile. Unlike Black's equation, once temperature, current, and geometry are specified, the TTF distribution is directly computed without per-geometry re-fitting. The EM techfile records the maximum current limits for metal lines with varying widths under the conditions of T_{ref} , CDF_{ref} and EOL_{ref} and adjustment factors as follows [14]:

$$I_{EM,limit} = I_{EM,ref} \cdot AF_T \cdot AF_{CDF} \cdot AF_{EOL} \tag{5}$$

$$AF_T = \exp\left[\frac{E_a}{kn}\left(\frac{1}{T_{EM}} - \frac{1}{T_{ref}}\right)\right] \tag{6}$$

$$AF_{CDF} = \exp\left\{\frac{\sigma}{kn}\left[\Phi^{-1}(CDF_{app}) - \Phi^{-1}(CDF_{ref})\right]\right\} \tag{7}$$

$$AF_{EOL} = \left(\frac{EOL_{ref}}{EOL_{app}}\right)^{\frac{1}{n}} \tag{8}$$

Here AF_T, AF_{CDF} and AF_{EOL} are the adjustment factors of T, CDF and EOL respectively. E_a, k, n are the EM activation

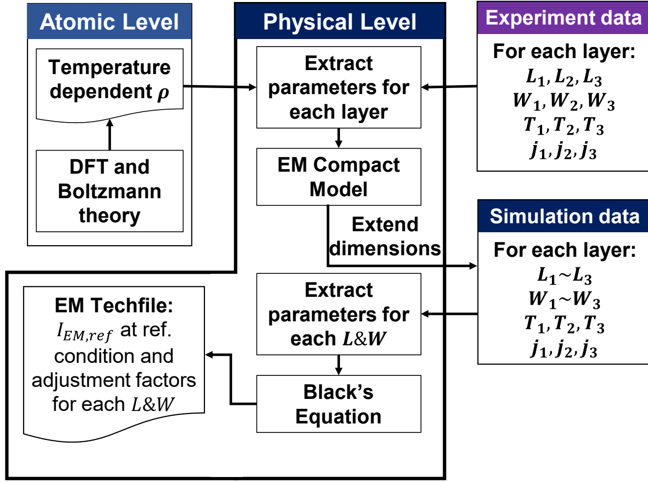


Fig. 4. EM techfile extraction flow.

energy, Boltzmann's constant and current exponent in Black's equation. Φ^{-1} is the inverse CDF and σ is the lognormal TTF standard deviation. Typically, the EM tech. profile provided by a fabrication specifies $I_{EM,ref}$ for only two line length: standard lines and short lines (with 20μm as the boundary). Because EM is length-dependent, extracting $I_{EM,ref}$ for every length via Black's equation alone is costly. Since the length effect is embedded in the compact model [17], it is easy to extend the EM techfile to entire length range using this model.

Fig.4 shows the EM techfile extraction flow, which extends dimensions from limited measurements (e.g. $L_{1,2,3}$= 9, 100, 500 μm, $W_{1,2,3}$ = 20, 100, 400 nm) via EM compact model. After extracting parameters, the EM compact model can extend simulation data for each $L\&W$. For each $L\&W$, adjustment factors and $I_{EM,ref}$ at reference condition are calculated through Black's Equation. This procedure allows for significantly reducing experimental measurements.

C. Multiscale Thermal Simulation

Because EM is exponentially sensitive to temperature, accurate thermal simulation of the chip is crucial. Traditional FEM solutions of the steady-state heat equation are too slow and memory-intensive for in-design P&R. We therefore adopt a 3D thermal resistor-network formulation and solve it with a GPU-accelerated, Kirchhoff's Current Law (KCL)-based iterative solver, which is lightweight enough to be invoked repeatedly during P&R process. As in Fig.5, the simulator takes as inputs the thermal-conductivity map, power map, detailed geometry, and boundary conditions from the layout. To handle the large thickness disparity across BEOL layers, we normalize the z-thickness to 100 nm and accordingly rescale in-plane and cross-plane conductivities, preserving the effective thermal resistances in all directions. We also use layer-dependent spatial resolution. The conductivity/power fields are then converted to an equivalent thermal-resistance network with distributed heat sources, and the temperature field for each layer is obtained via parallel KCL iterations.

Fig.6 shows how the multiscale thermal simulation model is integrated into P&R process. During placement, macro since signal routing is not yet available, we only consider the interconnects between FEOL and PDN. This assumption is valid because the highest temperature regions calculated under this assumption are consistent with those obtained when signal

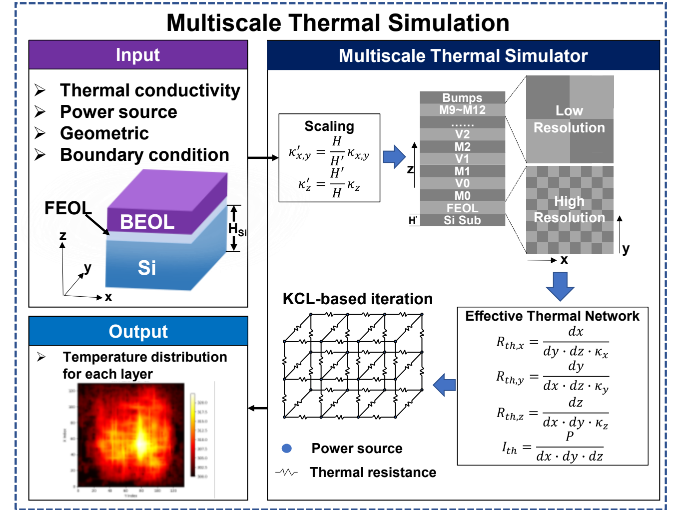


Fig. 5. Multiscale thermal simulation method based on physical multiscale thermal simulator.

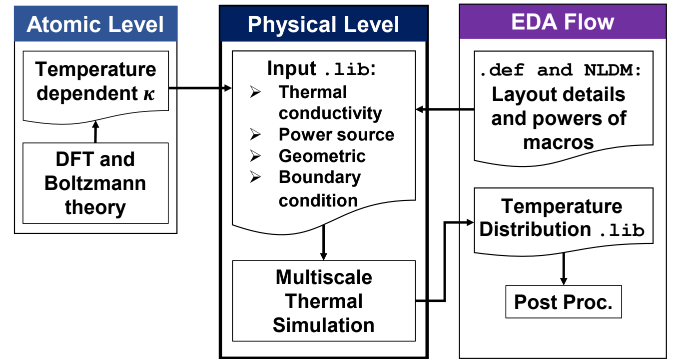


Fig. 6. The flow of multiscale thermal simulation for P&R.

lines are considered. At the routing phase, signal lines are added with the same flow. The effective FEOL thermal conductivity is set to 10.7W/(m·K) [20] and the copper conductivity is obtained from DFT. Once the input `.lib` is prepared, the simulator runs and outputs layer-wise temperature maps, for EM optimization in P&R stages.

D. EMaper-placer: EM-aware Placement

We propose an EM-aware global placement (GP) framework that integrates cell power into the placement optimization process by leveraging the physical analogy between thermal diffusion and electrostatics. Traditionally, GP is formulated as a wirelength minimization problem with a density penalty D_ρ:

$$\min_{v} WL(\boldsymbol{v}) + \lambda_\rho D_\rho(\boldsymbol{v}) \quad (9)$$

By analogy, D_ρ can be viewed as electrostatic energy induced by cell area density, described by Poisson's equation [21]:

$$\nabla^2 \phi(x, y) = -\rho(x, y) \quad (10)$$

$$\begin{cases} \hat{n} \cdot \nabla\phi(x, y) = 0, \ (x, y) \in \partial R \\ \iint_R \rho(x, y) = \iint_R \phi(x, y) = 0 \end{cases} \quad (11)$$

However, conventional density constraints focus on overlap avoidance and rarely account for power or its EM impact. Small-area, high-static-power cells can cluster without violating density, creating localized EM risk in the power grid. To address this, we introduce a power-aware constraint:

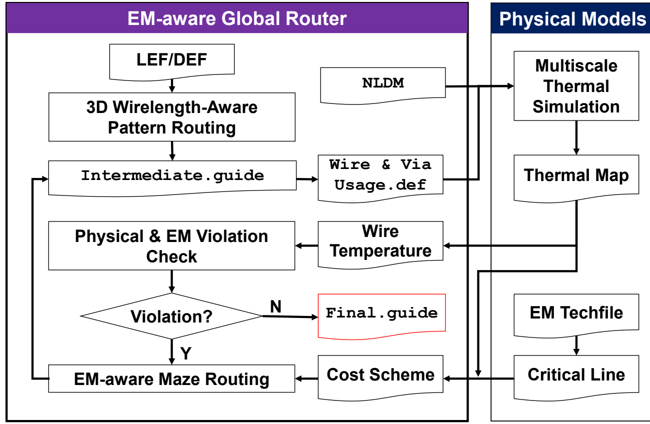


Fig. 7 Emaper-router: EM-aware global router incorporating physical models

$$\min_{v} WL(v) \ \text{s.t.} \begin{cases} \rho_b(v) < \rho_t \\ p_b(v) < p_t \end{cases} \tag{12}$$

Here p_b denotes the power-density map. The relaxed objective becomes:

$$\min_{v} WL(v) + \lambda_\rho D_\rho(v) + \lambda_p D_p(v) \tag{13}$$

Here, D_p is a novel power penalty inspired by heat conduction. In steady state, temperature T obeys the diffusion equation:

$$k\nabla^2 T(x,y) = -Q(x,y) \tag{14}$$

with thermal conductivity k and power density Q. This shares the same form as Poisson's equation, so T plays the role of a "potential" induced by power; minimizing the "energy" spreads high-power cells and reduces EM-prone hotspots.

Based on this analogy, we build a unified scheme where cell area and power are jointly encoded into a Poisson-based potential field to guide placement. We implement this by extending the open source global placer DREAMPlace [22]: we incorporate a power-aware density map into its existing Poisson solver and use its automatic differentiation for forward/backward of the combined density cost. Final detailed placement is performed using ABCDPlace [23].

E. EMaper-router: EM-aware Routing

Building on our physics-informed flow, we extend EM reliability to the routing stage with a focus on signal wires. As shown in Fig.7 EMaper-router integrates EM models into both pattern routing and maze routing. After each routing iteration, the intermediate layout is fed to the thermal simulator to generate a chip-wide temperature map, which then guides the next maze-routing pass forming a closed-loop thermal-aware optimization. The implementation is built upon the open source CUGR [24] with Dr.CU [25] for detailed routing.

We first use FLUTE to decompose nets into two-pin pairs (preprocessing). Pattern routing then follows CUGR's dynamic-programming (DP) formulation for Steiner subtrees. However, conventional L-shape patterns (Fig. 8a) can violate EM limits when one leg exceeds a critical length. We therefore introduce a wirelength-aware pattern (Fig. 8b): any over-length leg $l > l_{th}$ is split into $n = \text{ceil}(l/l_{th})$ segments with adjacent segments assigned to different metal layers. The DP cost is augmented to consider these segmented multi-layer patterns, so the optimal subtree naturally prefers EM-safe segment lengths while balancing wirelength and via overhead. After pattern routing we use extracted wire/via usage to drive

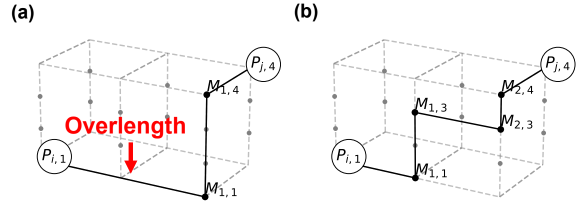


Fig. 8. (a)L-shape pattern routing (b) Wirelength aware pattern routing

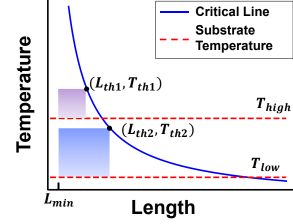


Fig. 9. Critical line and safe region used to determine EM thresholds.

Algorithm 1: EM-aware Maze Routing

Input: Grid graph G, pin set P, wirelength map W, length cost $f()$, start-pin accesses
Output: Routed Net

1 Initialize vertexCosts$[v]$ and priority queue Q
2 **while** *there exists an unvisited pin in* P **do**
3   **while** Q *not empty* **do**
4     $(c, u, \ell, \texttt{prev}, \texttt{isVia}) \leftarrow Q.\text{pop}()$
5   **if** u *is an unvisited pin* **then**
6   dstVertex $\leftarrow (c, u, \ell, \texttt{prev}, \texttt{isVia})$; **break**
7   **if** $c >$ vertexCosts$[u]$ **then**
8   continue
9   **foreach** *direction* d *in ValidDirections* **do**
10       $v \leftarrow \text{EdgeEnd}(u, d)$
11       $\texttt{nextVia} \leftarrow (d \in \{\text{UP}, \text{DOWN}\})$
12       $\ell_{\text{old}} \leftarrow \max(\ell, W[u])$
13       $\ell_{\text{new}} \leftarrow \max(\texttt{nextVia}?0 : \ell_{\text{old}} + \Delta\ell, W[v])$
14   **if** $c = 0 \wedge \ell \neq 0$ **then**
15         $c' \leftarrow c + \text{EdgeCost} + \text{TempCost} + f(\ell_{\text{new}})$
16   **else**
17         $c' \leftarrow c + \text{EdgeCost} + \text{TempCost} + f(\ell_{\text{new}}) - f(\ell_{\text{old}})$
18   **if** $c' <$ vertexCosts$[v]$ **then**
19         $Q.\text{push}(c', v, \ell_{\text{new}}, \texttt{prev} = u, \texttt{isVia} = \texttt{nextVia})$
20   `BacktraceAndUpdate`(dstVertex)
21 **return** *routed net*
22 **Function** `BacktraceAndUpdate`$((c, v, \ell, \textit{prev}, \textit{isVia}))$:
23   path $\leftarrow []$
24   **while** $v \neq$ *null* **do**
25   Append v to front of path
26     $v \leftarrow$ Prev$[v]$
27   finalPath $\leftarrow$ TryMerge(path, merged) ? merged : path
28   updateWireLengthMapForPath(finalPath)
29   addSegmentFromPath(finalPath)   `// use isVia[v] to cut segments`
30   **foreach** u *in finalPath* **do**
31   vertexCosts$[u] \leftarrow 0$
32     $Q.\text{push}(0, u, 0, \texttt{prev} = \textit{null}, \texttt{isVia} = \textit{false})$

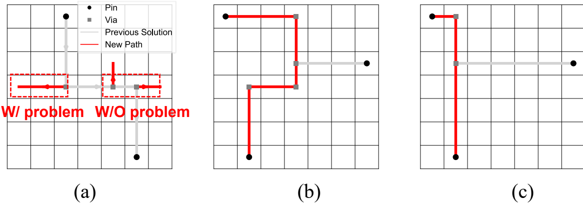
the multiscale simulator, with resulting temperature map identifies EM-risky nets to be ripped up and rerouted. Next, we perform a coarse-grained guide generation as in CUGR, but relax guide layer restrictions to enlarge the search space for the subsequent maze routing. Our EM-aware maze router extends Dijkstra algorithm with two exponential penalties:

$$\text{TempCost(e)} = C_T \exp[\beta_T(T_e - T_{th})] \tag{15}$$

$$\text{LengthCost}(e) = C_L \exp[\beta_L(L - L_{th})] \quad (16)$$

Where T_e is the edge(e)-local temperature, and L is the path - accumulated wire-length. We set (T_{th}, L_{th}) by a max-rectangle rule on the EM techfile's critical line: consider rectangles ("safe region") whose lower bounds are substrate temperature T_{sub} and L_{min} with upper-right corner lies on the critical line (Fig. 9). The safe region with the largest area gives T_{th} and L_{th}, yielding self-adaptive EM margins across mission profiles.

Since the temperature term is edge-local while the wirelength term is dependent on cumulative path information, we maintain per-node state $(u, c, p, l, isVia)$ in Algorithm 1 (node, cost, predecessor, wire-length, via flag). When l approaches L_{th}, the incremental cost rises sharply, encouraging layer switches to stay within EM-safe regimes. Upon reaching a target pin, we backtrack the route and register lengths. To correct length accounting under overlaps (Fig. 10(a)), we perform segment-wise merging (split at vias) against a global wirelength map W: matched segments are merged with a unified length; otherwise they are inserted as new segments. This yields more accurate length accounting and EM risk evaluation, as compared in Fig.10 (b) and (c).



(a) (b) (c)

Fig. 10. (a) Path w/ and w/o backtrack problem. (b) EM-aware maze routing result. (c). Result from baseline Dijkstra routing.

IV. Experiment Results

We implement EMaper in C++/Python and evaluate it on a workstation with an Intel Core i7-13700 (4.10 GHz), 32 GB RAM, and an NVIDIA RTX 4060. The NanGate 15 nm standard-cell library [27] is integrated with the ISPD-2018 benchmarks [28] to derive cell current and power.

A. Physical Model

For the atomic-level calculation, electron–phonon–limited relaxation times are computed using EPW code [29]. Fig.11(a) reports the relaxation time for Copper near the Fermi level, with averaged value $\tau_0 = 33.59$ fs. Using τ_0, temperature-dependent electrical and thermal conductivities are obtained with BoltzTrap2 [16] and VASP [30], as shown in Fig.11(b).

The EM compact model agrees well with experimental data across temperatures [31] (Fig. 12). We then generate an EM techfile for P&R covering width 20~400 nm and a length ranging from 9~500 μm, with reference conditions $CDF = 10^{-7}\%, T = 100\ °\text{C}$, and $EOL = 10^6$ h. As illustrated in Fig.13(a) and Fig.13(b), the extracted Black's Equation parameters—activation energy E_a and current exponent n—exhibit strong geometry dependence: both rise with L below $50\mu m$ and saturate beyond, and both also increase with W. Fig.13(c) demonstrates strong compatibility with Black's equation. Critical curves at fixed width (e.g., 30 nm) are extracted for multiple current levels (Fig. 13(d)) and used by the EM-aware routing flow.

B. EM-Aware EDA Flow

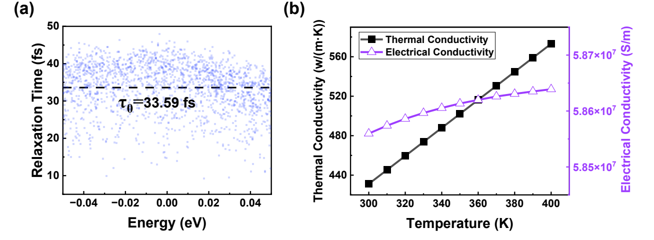


Fig. 11. (a) The relaxation time of electrons near the fermi energy(0 eV) and average value. (b) The electrical and thermal conductivity at different temperature

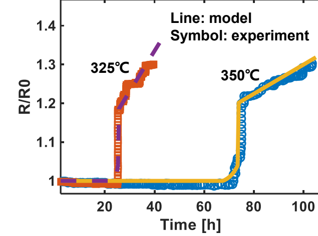


Fig. 12. Comparison of the EM compact model with experimental data

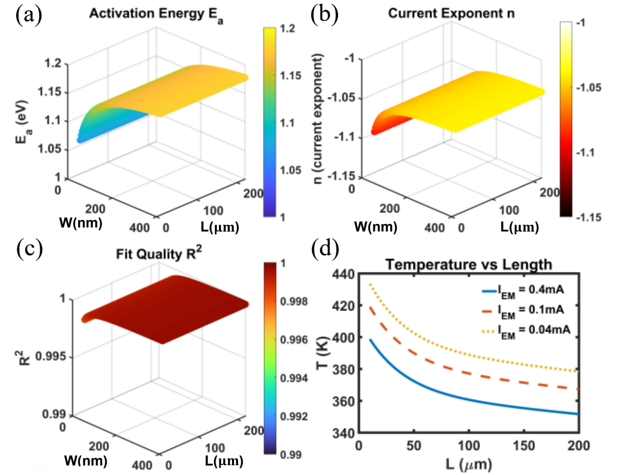


Fig. 13. Parameters extracted in Black's Equation: (a) Activation Energy E_a, (b) current exponent n, (c) fit quality R^2, (d) Temperature-length curve for different I_{EM}.

We take the ispd18_test1 benchmark to visualize how EMaper-placer improves PDN EM reliability. Fig.1 compares temperature maps after placement by DREAMPlace vs EMaper-placer using our multiscale thermal simulator. EMaper-placer spreads power to suppress hotspots, reducing T_{max} from 124.02 °C to 108.11 °C (-15.91 K) with only a 10% increase in wirelength (wHPWL) —a favorable trade-off for EM reliability. Dynamic IR-drop evolution from our EM compact model is shown in Fig. 15. Under DREAMPlace, uneven power concentrates heat and accelerates EM, driving the max IR-drop from 30.04 mV(fresh state) to 40.09 mV (100 000 power-on hour, +33 %). With EMaper-placer, power sparsification balances current and suppresses hotspots; the IR-drop rises only 29.75 → 31.53 mV (+5.98 %). We then evaluate routing reliability via the temperature–wirelength distribution (Fig. 16). An intentionally stringent critical line from the EM techfile: $I_{EM} = 0.4$ mA, $W = 40$ nm, $CDF = 10^{-7}\%$, $EOL = 10^5$ h serves as the threshold; points above it are violations. With T_{sub}=350 K, the baseline router (CUGR) exhibits several violations, whereas EMaper-router eliminates them entirely. With T_{sub}=360 K, CUGR's violations rise markedly, while EMaper-router adapts to the

TABLE I: COMPARISION OF WIRELENGTH, #VIA AND #EM VIOLATION WITH DREAMPLACE & CUGR

Design	DREAMPlace+CUGR				EMaper				Rel.	
	WireLength	# via	WL&Via Score	# EM vio.	WireLength	# via	WL&Via Score	# EM vio.	WL&Via degradation	# EM vio.improve.
ispd18_test1@300K	448268	31649	287432	0	448268	31649	287432	0	0%	-
ispd18_test1@350K	448268	31649	287432	18	473085	31894	300330	0	4.49%	100%
ispd18_test1@360K	448268	31649	287432	100	494455	34045	315317	1	9.70%	99%
ispd18_test2@300K	7610010	299719	4404443	0	7610010	299719	4404443	0	0%	-
ispd18_test2@350K	7610010	299719	4404443	2541	8450570	331830	4888943	6	11.0%	99.7%
ispd18_test2@360K	7610010	299719	4404443	4740	8705620	385245	5123300	373	16.3%	92.1%

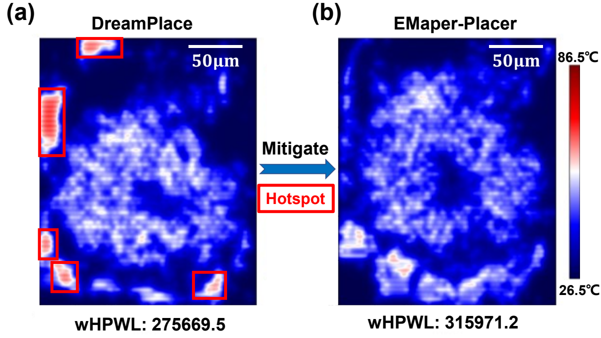


Fig. 14. Temperature map of ispd18_test1 after placement: (a) DreamPlace, (b) EM-aware Placer.

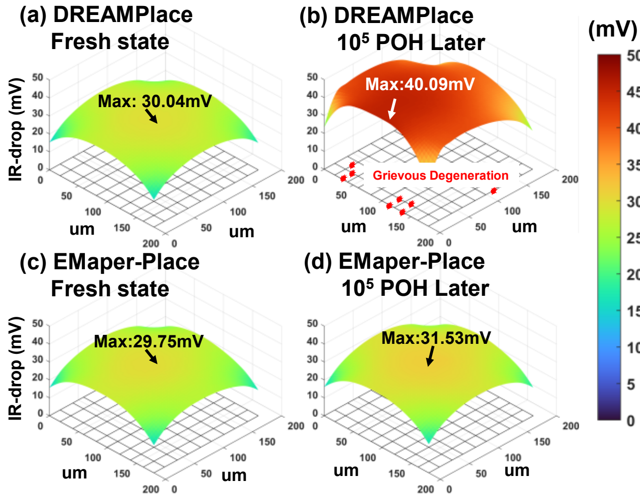


Fig. 15. IR-drop map of ispd18_test1 after placement: (a) fresh state by DREAMPlace, (b) 100 000 POH later by DREAMPlace, (c) fresh state by EMaper-placer, (d) 100 000 POH later by EMaper.

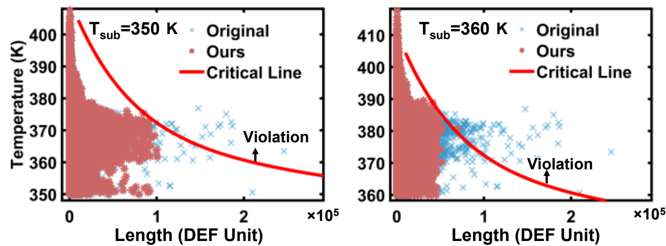


Fig. 16. Wirelength–temperature distribution of Emaper-router and CUGR (Original) under two temperature conditions: (a) 350K. (b) 360K

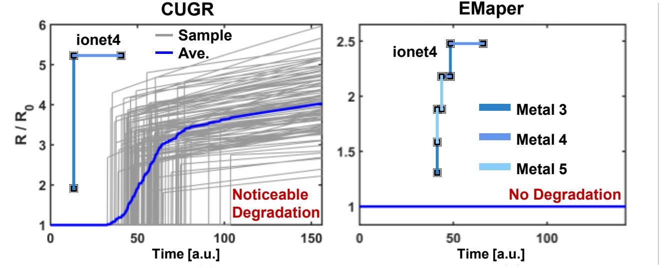


Fig. 17 Resistance trace of ispd18_test2 innet4 under CUGR and EMaper.

substrate temperature and the techfile-derived critical line, maintaining robust reliability. We take a segment of ionet4 in ispd18_test2 to demonstrate the EM improvement. Time-dependent resistance traces (Fig. 17) highlight the mechanism: at T_{sub}=350K CUGR's route contains a long segment and exhibits resistance growth, while EMaper-router splits the path into safer segments, showing no observable degradation.

To further validate our workflow, we conduct experiments on the ispd18 benchmark suite under multiple mission profiles. we compare wirelength (WL), via count (#via), and the number of EM violations (#EM vio) against a baseline (DREAMPlace + CUGR), as shown in Table 1. WL and via count remain comparable in most cases. At 300 K, both flows are identical, indicating that our self-adjusting framework introduces no unnecessary cost under benign conditions. At higher temperatures, EMaper-router reduces violations substantially: on ispd18_test1@350 K, it eliminates 100% EM violations with only +4.49% overhead; on ispd18_test2@360 K, it eliminates 92.1% violations at +16.3% overhead—an advantageous trade-off for mission-profile–aware EM reliability.

V. CONCLUSION

In this work, we propose EMaper, a cross-level EM-aware physical design framework that integrates physics-informed compact modeling, multiscale thermal simulation, and early-stage placement and routing co-optimization. Unlike traditional post-layout EM verification flows, EMaper performs in-design prediction and mitigation of EM risks by embedding mission-profile-aware constraints into the physical design process. Experimental results on the ISPD18 benchmark suite under multiple operating scenarios demonstrate that EMaper eliminates 92.1% to 100% of EM violations, with wirelength and via count overhead limited to 4.49% to 16.3%. In thermally benign conditions, EMaper naturally incurs zero overhead, showcasing its self-adaptive optimization capability. These results confirm the effectiveness and practicality of EMaper as a scalable and reliability-driven solution for thermally aware physical design in advanced VLSI systems.

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