IR Drop-Aware ECO: A Fast Approach to Minimize Layout and Timing Disturbance

Jingchao Hu*, Yibo Lin†, Hao Yu‡, Quan Chen‡, Zhou Jin*§, Cheng Zhuo*
* College of Integrated Circuits, Zhejiang University, Hangzhou, China
† School of Integrated Circuits, Peking University, Beijing, China
‡ School of Microelectronics, Southern University of Science and Technology, Shenzhen, China
§ Corresponding author e-mail: z.jin@zju.edu.cn

***Abstract*—Ensuring power integrity in advanced IC design is increasingly challenging, as excessive IR drop can severely impact circuit performance and reliability, especially during the late-stage Engineering Change Order (ECO) process. In this work, we propose a novel IR drop-aware ECO framework that addresses IR drop violations through targeted cell displacement while minimizing timing and layout disruption. Our approach incorporates vertical IR drop mitigation and horizontal timing fix, and employs a rail severity scoring mechanism that combines current correlation and spatial proximity to evaluate IR drop severity. Experimental results on three post-routed benchmark designs demonstrate that our method achieves significant reductions in worst-case dynamic voltage drop for certain designs and mitigates local timing degradation. Additionally, the proposed severity score accurately reflects trends in IR drop risk, providing valuable guidance for ECO optimization.**

***Index Terms*—IR-Drop, ECO, Timing, Cell Displacement**

I. Introduction

As technology nodes continue to shrink, power integrity has become a critical factor affecting chip performance [1]–[6]. Among various power-related issues, IR drop has a significant impact on the functionality and reliability of modern integrated circuits. Specifically, IR drop weakens transistor drive capability, increases gate and interconnect delays, and amplifies clock uncertainty, all of which contribute to reduced timing margins. In severe cases, IR drop may even induce setup/hold violations and functional errors.

It is important to note that while IR drop and timing violations are both crucial concerns, their underlying causes differ: IR drop is primarily induced by excessive current or large effective resistance in the power delivery network, whereas timing violations usually originate from logic depth or other design factors. Nevertheless, IR drop and timing are highly coupled in practice. As a result, any mitigation technique aimed at reducing IR drop must be carefully coordinated to avoid compromising timing performance [7], [8], since unintended timing degradation can offset the benefits gained from IR drop correction.

In late-stage design, these coupled challenges are typically addressed through ECO, a process used to correct remaining issues after the main design has been finalized. The key objective of ECO is to make minimal adjustments while ensuring that the design meets the required constraints, such as timing, power, and signal integrity. Common techniques for correcting IR drop during the ECO phase include cell relocation, buffer insertion, and cell resizing.

During the ECO phase, timing is typically close to closure, with only a few marginal violations remaining and timing margins unevenly distributed. However, dynamic IR drop hotspots may still exist, particularly in regions with high switching activity or significant effective resistance in the power network. The main challenge at this stage is to correct the IR drop hotspots without degrading the timing. In other words, the changes made during ECO to address IR drop must not introduce significant timing regressions, as timing is already on the edge of closure.

Several recent studies have proposed methods for improving IR drop correction during the ECO phase. For example, [9] introduces a hybrid ECO detailed placement flow aimed at reducing dynamic IR drop, while [7] leverages cell movement and current waveform staggering combined with machine learning guidance to mitigate peak current. Despite the progress, these methods still have one limitation: minimizing total displacement as an indirect way of reducing timing impact is insufficient, as the timing sensitivities of different cells may vary significantly. The same amount of movement may have a vastly different effect on critical and non-critical paths.

In this paper, we propose a timing-aware IR drop ECO framework that explicitly considers timing constraints during the optimization process. By integrating timing-critical path identification and weighted net optimization into cell displacement and legalization, our approach mitigates IR drop while reducing adverse timing impact. Our contributions are summarized as follows:

- **A timing-aware legalization and optimization strategy.** After IR drop optimization, we introduce a targeted timing fix and cell legalization process, which identifies critical timing paths within the ECO region, assigns composite net weights, and minimizes both average cell displacement and weighted net wirelength changes. By incorporating restricted swapping and non-overlapping constraints, this approach ensures robust timing closure with minimal disturbance to the existing layout.
- **A quantitative rail severity scoring mechanism based on current and spatial correlation.** We propose a novel scoring system that evaluates the severity of IR drop

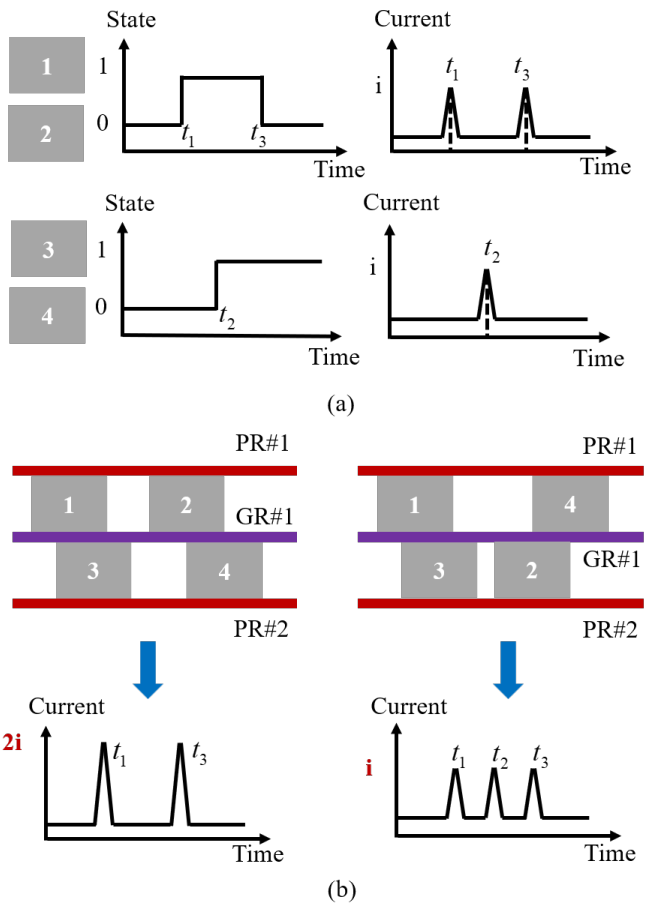

Fig. 1. (a) The state switching behavior and current waveforms on the VDD pins of $cell_{1\to4}$; (b) The current waveform observed at VDD_1 before and after swapping $cell_2$ and $cell_4$.

risk by measuring the temporal correlation of current waveforms and the spatial proximity of cells sharing the same power/ground rail. This metric can predict the effectiveness of IR drop mitigation before performing full dynamic voltage drop analysis.

We apply our method to three post-routed designs. For the `aes` design, our approach achieves a substantial reduction in worst-case dynamic voltage drop (DVD) by over 50 mV, while also mitigating local timing degradation. Furthermore, the proposed IR drop severity score accurately tracks trends in worst-case DVD improvements, confirming its utility for risk assessment and optimization guidance.

II. Background and Preliminaries

A. Staggering of peak current on the same power rail

Addressing IR drop violations is a critical challenge during the post-routing ECO phase. Although several effective techniques exist, including useful skew scheduling [10], adding power stripe connections [11], and cell resizing [12], this work specifically investigates cell displacement [7], [9] as a primary strategy for IR drop mitigation. One such cell displacement technique is staggering [7], which aims to reduce the peak current on a power rail by offsetting the current waveforms of cells that share it. This desynchronization lowers the aggregate peak current drawn from the rail, thereby mitigating dynamic IR drop. An example is shown in Fig. 1. Initially, $cell_1$ and $cell_2$ are placed on the same power rail VDD_1 and share the same switching time t_1. Each cell draws a peak current of i at t_1. Meanwhile, $cell_4$ (located on a different rail) switches at a different time t_2. Due to the simultaneous switching of $cell_1$ and $cell_2$, the amplitude of the aggregate peak current observed at VDD_1 is $2i$, which can lead to IR drop violations. However, if we swap the positions of $cell_2$ and $cell_4$, the cells on VDD_1 are now $cell_1$ (switching at t_1) and $cell_4$ (switching at t_2). The peak current timings on VDD_1 are now staggered. This staggered switching significantly reduces the maximum peak current on VDD_1 from $2i$ down to i, thereby mitigating IR drop, particularly dynamic Ldi/dt effects. The linear superposition of instance-level VDD pin currents onto the aggregate power rail current is what enables this efficient optimization.

B. Timing-Driven Cell Placement

Timing-driven placement is a key technique in physical design, aiming to meet circuit timing constraints through strategic cell placement. Two mainstream approaches are widely used: net-based and path-based timing-driven placement.

Net-based methods [13]–[15] focus on optimizing the delays of individual timing-critical nets. In these approaches, each net is assigned a weight that reflects its timing importance, typically derived from static timing analysis. During placement, the algorithm adjusts the positions of cells to minimize the weighted sum of net delays, thereby reducing the delay on those nets that are most likely to affect circuit timing. Net-based methods are computationally efficient and can be easily integrated into standard placement flows, making them widely adopted in industry. However, because they treat nets independently, they may not accurately capture cumulative timing effects along multi-stage critical paths.

Path-based methods [16], [17], by contrast, directly target the timing of entire critical paths. Instead of focusing on single nets, these methods treat each critical path as an integrated optimization object, considering the combined delay of all cells and nets along the path. The optimization objective is often to minimize the maximum or total delay across all critical paths, which can lead to more accurate timing improvement—especially for designs with deep or complex timing paths. Path-based approaches may employ mathematical programming, such as linear programming or Lagrangian relaxation, to enforce overall path timing constraints during placement. While offering higher timing accuracy, these methods are typically more computationally intensive.

In this work, inspired by traditional net-based or path-based placement optimization, we propose a timing-aware legalization strategy tailored for the ECO process. Our approach first identifies critical timing paths within the ECO region and assigns composite weights to the relevant nets. During legalization, we minimize both the cell displacement and the

weighted changes in net wirelength, ensuring that IR drop mitigation is achieved while counteracting timing degradation.

III. IR-Drop aware cell displacement ECO

A. ECO Region Definition

Similar to the approach in [7], we divide the entire PDN region into several bins. However, unlike [7], our division is based on well-tap cells, as shown in Fig. 2. This approach fully leverages the fact that well-tap cells and standard cells are placed at the same hierarchical level and are evenly spaced. This avoids the issue that may arise when dividing bins based on vias, where it becomes difficult to determine the bin assignment when a cell overlaps with a via.

All bins containing hotspots will be identified. Among these bins, those that are spatially adjacent will be merged into a larger region. Finally, we will obtain several regions that are not spatially adjacent to each other, which we define as the ECO regions.

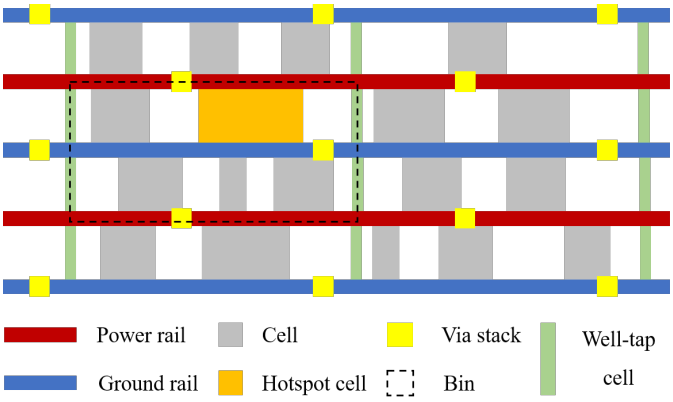

Fig. 2. Bin division based on well-tap cells.

B. Row Assignment for Cells

As stated in Section II, the peak current observed from the power/ground rails can be reduced to alleviate the dynamic IR drop issue by staggering the times at which the peak currents of the VDD pins of instances sharing the same rail occur. Since the total current observed by a power/ground rail is simply the linear sum of the currents on the VDD/VSS pins of the cells connected to it, Integer Linear Programming (ILP) is employed to address the minimization of this peak current. The relevant notations are defined in Table I, and the objective as well as the constraints are formulated following the works in [9] and [7].

The objective of the ILP in this stage is to minimize the peak current on the power/ground rail by optimally staggering the switching times of the VDD pins [7]:

$$Min(Max^P + Max^G) \tag{1}$$

TABLE I
Design-related parameters and variables used in ILP for peak current minimization.

Parameters	
Name	**Description**
N	Integer. Number of power rails in an ECO region.
T	Number of total timesteps in selected VCD segments.
K	Number of standard cells in an ECO region.
C	The set of standard cells in an ECO region. $C = \{c_1, c_2, ..., c_K\}$.
W	$W[i]$ is the width of cell c_i.
S	$S[j]$ is the capacity of j^{th} row.
I^P	$I^P[i,t]$ is the current on VDD pin of cell c_i at timestep t.
I^G	$I^G[i,t]$ is the current on VSS pin of cell c_i at timestep t.
B^P	$B^P[j,t]$ is the background noise of the j^{th} power rail at time step t.
B^G	$B^G[j,t]$ is the background noise of the the j^{th} ground rail at time step t.
Variables	
Max^P	Continuous variable. Maximum peak current among all power rails.
Max^G	Continuous variable. Maximum peak current among all ground rails.
$r_{i,j}$	Binary variable. $r_{i,j} = 1$ if c_i located at the j^{th} row.
$p_{i,j}$	Binary variable. $p_{i,j} = 1$ if c_i aligns to the j^{th} power rail.
$g_{i,j}$	Binary variable. $g_{i,j} = 1$ if c_i aligns to the j^{th} ground rail.

in which Max^P, Max^G meets

$$\begin{aligned} B^G[j,t] + \sum_{i=1}^{K} g_{i,j} I^G[i,t] \le Max^G, \\ B^P[j,t] + \sum_{i=1}^{K} g_{i,j} I^P[i,t] \le Max^P \end{aligned} \tag{2}$$

for all power/ground rails and time steps.

To reduce the extent of layout perturbation, each cell is restricted to move at most 3 rows up or down from its original row.

C. Timing Fix and Cell Legalization

To further minimize the timing impact introduced by vertical cell movements in the previous optimization stage, we introduce an additional horizontal displacement step. By carefully adjusting cell positions along the horizontal direction, we can effectively compensate for any adverse effects on timing, thus achieving a finer balance between IR drop mitigation and timing closure. Such horizontal adjustments help restore or improve timing characteristics that may have been degraded, with minimal disruption to the overall layout.

Building upon the previous optimization results, we further address timing closure and placement legalization through a targeted and efficient process.

1) Critical Path Selection and Net Weight Assignment: For each ECO region, we first collect the timing paths that traverse the region and have the worst slack, as these are most sensitive to timing degradation. To ensure a diverse and representative selection, we sort these candidate paths in two

ways: (1) by timing slack, and (2) by a combined metric that considers both the path length and the number of instances on the path that overlap with instances in the ECO region. Paths are then alternately selected from these two sorted lists and added to the final set of critical paths, until the total number of selected paths reaches α.

Let $\mathcal{P} = \{p_1, p_2, ..., p_\alpha\}$ denote the set of selected critical paths, and let $\mathcal{N}_\mathcal{P}$ be the set of nets appearing on these paths. For each net $n \in \mathcal{N}_\mathcal{P}$, we assign a composite weight w_n reflecting both timing criticality and electrical characteristics:

For the timing-related part of the net weight, we define the weight for each net n (associated with path p) as

$$w_{\text{slack},n} = 1 + \max\left(0, (s_{\min} - s_p + t_0) \cdot \gamma\right) \tag{3}$$

where $s_{\min}$ is the minimum slack among all selected critical paths, s_p is the slack of path p, t_0 is a slack threshold that controls the sensitivity to slack differences, and γ is a scaling factor that adjusts the influence of slack on the net weight.

For the driver resistance component, the weight for each net n is defined as

$$w_{\text{drv},n} = 1 + 0.01 \cdot r_n \tag{4}$$

where r_n is the driver resistance of net n.

The total net weight is then given by:

$$w_n = w_{\text{slack},n} \cdot w_{\text{drv},n} \tag{5}$$

2) HPWL Change Calculation:

For each net, we calculate the change in Half-Perimeter Wire Length (HPWL) before and after cell movement. The HPWL of a net is defined using the bounding-box model:

$$\text{HPWL}(n) = (x_{\max} - x_{\min}) + (y_{\max} - y_{\min}) \tag{6}$$

where $x_{\max}$, $x_{\min}$, $y_{\max}$, and $y_{\min}$ are the maximum and minimum x and y coordinates among all pins of net n.

The weighted sum of HPWL changes is then computed as

$$\Delta_{\text{HPWL}} = \sum_{n \in \mathcal{N}_\mathcal{P}} w_n \cdot (\text{HPWL}_{\text{new}}(n) - \text{HPWL}_{\text{orig}}(n)) \tag{7}$$

3) Legalization and Feasibility Constraints:

To ensure legal placement and reduce layout perturbation:

- **Non-overlap:** No two instances are allowed to overlap after displacement.
- **Restricted swapping:** Within each placement row, the relative order of instances is preserved except that each instance is allowed to swap position only with its immediate left or right neighbor. This restriction significantly simplifies legalization and limits overall layout disturbance.

4) Optimization Objective:

The final optimization objective is to minimize a composite cost comprising average cell displacement and the weighted, normalized HPWL change:

$$\text{Cost} = \frac{1}{N_{\text{inst}}} \sum_{i=1}^{N_{\text{inst}}} |\Delta x_i| + \beta \frac{1}{|\mathcal{N}_\mathcal{P}|} \cdot \Delta_{\text{HPWL}} \tag{8}$$

where N_{inst} is the total number of instances considered, Δx_i is the displacement of instance i, and β is a scaling parameter balancing placement stability and timing-driven wire length optimization. The timing fix and cell legalization steps are also formulated and solved using ILP models.

This approach ensures that the timing fix and cell legalization process is both timing-aware and minimally invasive, providing robust timing closure while reducing unnecessary layout modifications.

IV. Current and Spatial Correlation Based Rail Severity Scoring

The severity of IR drop violations within a design region is closely related to the temporal and spatial relationships among instances sharing the same power/ground rail. To compare the quality of IR drop before and after ECO without performing a full DVD analysis, we propose this severity score based on current correlation and spatial correlation between cell pairs.

1) Current Correlation:

When multiple instances on the same power rail draw peak current simultaneously, the aggregate instantaneous current increases, leading to a larger IR drop. The concept of *staggering* current waveforms—introduced previously—aims to intentionally desynchronize the peak current timings of such instances to reduce the likelihood of simultaneous surges. To quantitatively capture how likely two instances are to have overlapping current peaks, we define the *current correlation* between two instances i and j as

$$\text{Corr}_c(i, j) = \mathbf{I}_i^\top \mathbf{I}_j \tag{9}$$

where $\mathbf{I}_i = [I_i(1), I_i(2), \ldots, I_i(T)]$ is the current waveform vector of instance i over T time steps. A higher value of $\text{Corr}_c(i, j)$ indicates that instances i and j are more likely to experience peak currents at the same time, and thus benefit more from waveform staggering. Moreover, a larger correlation value may also reflect that either instance i or j individually has a larger current magnitude.

2) Spatial Correlation:

The physical proximity of instances with high current correlation further exacerbates IR drop issues. When two such instances are placed close to each other on the same power rail, their simultaneous current draw can result in significant localized voltage drop. We define the *spatial correlation* between two instances as

$$\text{Corr}_s(i, j) = \frac{1}{1 + |x_i - x_j|} \tag{10}$$

where x_i and x_j denote the physical coordinates (e.g., along the x-axis) of instances i and j on the same power rail. The smaller the distance, the higher the spatial correlation.

3) Rail Severity Score:

To capture the overall IR drop risk associated with each individual power or ground rail within a region, we define a rail severity score that aggregates pairwise interactions for each rail. Specifically, for each rail r (including both power and ground rails) in the region, we compute the severity score

as the sum of the products of current correlation and spatial correlation over all distinct pairs of instances aligned to that rail:

$$\mathcal{S}_r = \sum_{\substack{i,j \in \mathcal{C}_r \\ i \neq j}} \left(\mathrm{Corr}_c(i,j) \cdot \mathrm{Corr}_s(i,j) \right) \tag{11}$$

where $\mathcal{C}_r$ is the set of instances aligned to rail r.

The overall severity score for the region is then defined as the maximum rail severity score across all power and ground rails in the region:

$$\mathcal{S}_{\text{region}} = \max_{r \in \mathcal{R}} \mathcal{S}_r \tag{12}$$

where $\mathcal{R}$ denotes the set of all power and ground rails in the region.

We further define a severity score for each placement row to enable finer-grained analysis. For a given row, we first identify its corresponding power and ground rails, then compute the row severity score as the sum of the severity scores of these two rails:

$$\mathcal{S}_{\text{row}} = \mathcal{S}_{\text{power rail}} + \mathcal{S}_{\text{ground rail}}. \tag{13}$$

A row with a higher $\mathcal{S}_{\text{row}}$ tends to exhibit a higher risk of IR drop, as it indicates the presence of strongly correlated instances both temporally and spatially on the associated power and ground rails. This row-level metric reflects the effective supply voltage experienced by the instances on that row, as it captures the combined effects of VDD IR drop and VSS ground bounce.

V. Experiment Results

Our experiments are conducted on three post-routed benchmark designs, each generated using the industrial-like flow illustrated in Fig. 3. The RTL source codes for these benchmarks are obtained from the OpenCores [18] project, and design details are summarized in Table II. Logic synthesis is performed in Cadence Genus targeting the open-source ASAP7 PDK [19], followed by placement and routing in Cadence Innovus to obtain final post-routed layouts. For dynamic IR-drop analysis, testbenches are simulated in VCS to generate VCD activity traces, with the number of time steps set to 1,000. All experiments are implemented in Python and executed on an Ubuntu 22.04 server equipped with an Intel Xeon Platinum 8475B (48 cores, 3.8GHz) and 503GB RAM, using Gurobi [20] as the ILP solver. In our experiments, the parameters α, β and γ are set to 500, 5e-3 and 20.

For each design, we select the 1,000 and 2,000 instances with the worst IR drop to define ECO regions. We then apply our IR drop-aware ECO framework and compare the resulting worst-case DVD after ECO, both with and without the timing fix, as summarized in Table III. The results show that our method significantly reduces the worst DVD for the `aes` design, achieves moderate improvement for `sha`, but has limited or even negative effects for `des`. This suggests that the effectiveness of IR-drop mitigation is dependent on the spatial and temporal distribution of peak currents across the shared power rails in each design.

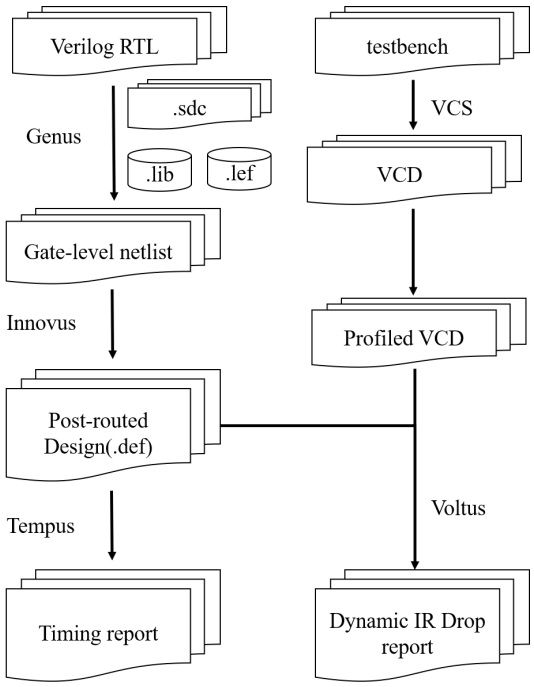

Fig. 3. Benchmark design generation flow.

TABLE II
Summary of Benchmark Designs and Their Instance Counts Used in Experimental Evaluation.

Design	`aes`	`des`	`sha`
#Insts	16,525	53,829	23,404

TABLE III
Comparison of Worst DVD and Average Displacement for Each Design under Different ECO Strategies. "Original" refers to the baseline design, "ECO" denotes IR-drop-aware cell displacement, and "ECO+T" includes additional timing fix.

Design	#Insts	Worst DVD (mV)			Avg disp. (um)	
		Original	ECO	ECO+T	ECO	ECO+T
`aes`	1K	130.97	72.80	78.38	139	1.52
	2K		68.34	60.81	1.44	1.80
`des`	1K	77.48	78.99	79.08	1.55	1.56
	2K		79.33	79.33	1.45	1.46
`sha`	1K	46.19	46.04	46.03	0.37	2.30
	2K		46.20	45.88	1.31	1.76

TABLE IV
Comparison of Worst Slack (WS) in nanosecond and Number of Violated Timing Paths (NVP) for Each Design under Different ECO Strategies.

Design	#Insts	Original		ECO		ECO+T	
		WS	NVP	WS	NVP	WS	NVP
`aes`	2K	0.008	0	0.006	0	0.006	0
`des`	2K	0.000	0	-0.001	1	-0.001	1
`sha`	2K	0.000	0	0.000	0	-0.000	1

TABLE V
LOCAL WORST SLACK (WS) AND SEVERITY SCORE COMPARISON FOR EACH DESIGN UNDER DIFFERENT ECO STRATEGIES.

Local WS (ps)				
Design	#Insts	Original	ECO	ECO+T
aes	1k	212.40	210.10	211.90
	2k	7.84	5.54	5.74
Severity Score				
Design	#Insts	Original	ECO	ECO+T
aes	1k	318.1	267.2	264.5
	2k		278.0	278.1

Table IV presents the worst slack (WS) and the number of violated timing paths (NVP) for each design under the three ECO strategies. The data show that our approach introduces minimal timing disturbance: in all cases, the change in WS is less than 2 ps, and the NVP does not increase noticeably. This is attributed to our joint optimization of cell displacement and weighted net HPWL, as well as the observation that IR-drop hotspots generally do not overlap with timing-critical instances closely.

To further assess local timing and IR-drop risk, Table V reports the local worst slack (local WS) for all timing paths traversing the ECO region, alongside the average row severity score computed from the ten rows with the highest row severity scores (as defined in Section III, with current measured in milliamperes and distance measured in micrometer). The results demonstrate that timing-aware ECO (ECO+T) can further improve local WS by 0.1 to 1.8 ps compared to ECO without timing fix. Moreover, the severity score, which quantifies local IR-drop risk, consistently decreases in line with improvements in worst DVD, validating the effectiveness of our severity grading metric.

VI. CONCLUSION

In this paper, we propose a novel IR drop-aware ECO framework that addresses IR drop violations during the late-stage design process through targeted cell displacement, while explicitly minimizing timing and layout disturbance. Our method integrates vertical IR drop mitigation with a horizontal timing fix and employs a severity scoring mechanism that combines current correlation and spatial proximity to enable assessment of IR drop mitigation results without the need for full DVD simulation.

Comprehensive experiments on three post-routed benchmark designs demonstrate that our framework can significantly reduce worst-case DVD for certain design cases, with the aes design experiencing a reduction of over 50 mV, while maintaining negligible impact on global timing and resisting local timing slack degradation. The severity score we propose effectively tracks IR drop risk trends, providing actionable guidance for ECO optimization and risk assessment.

As future work, we plan to incorporate the severity score directly into the optimization process to further enhance the effectiveness of IR drop mitigation.

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