S^{3}DET: Detecting System Symmetry Constraints for Analog Circuit with Graph Similarity

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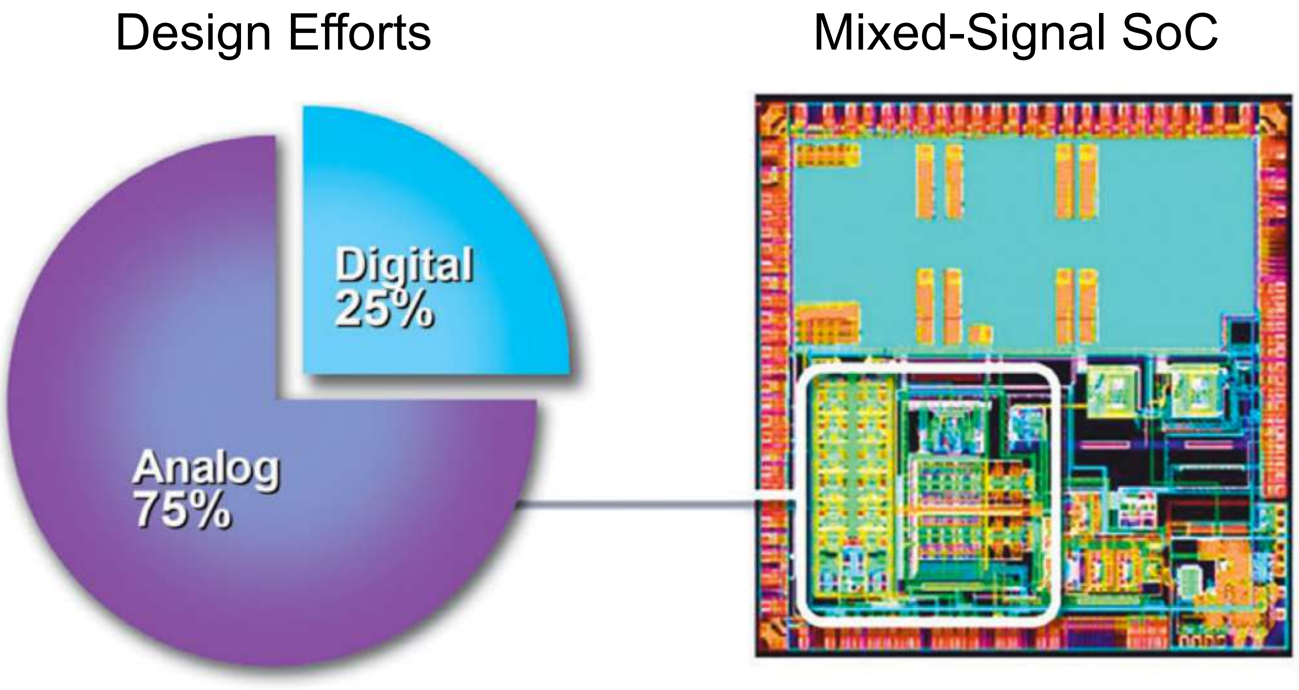
Analog/Mixed-Signal IC Design

- Typical modern SoCs:
  - Less than 25% total die area for analog; however, 75% or more design efforts



Design Efforts

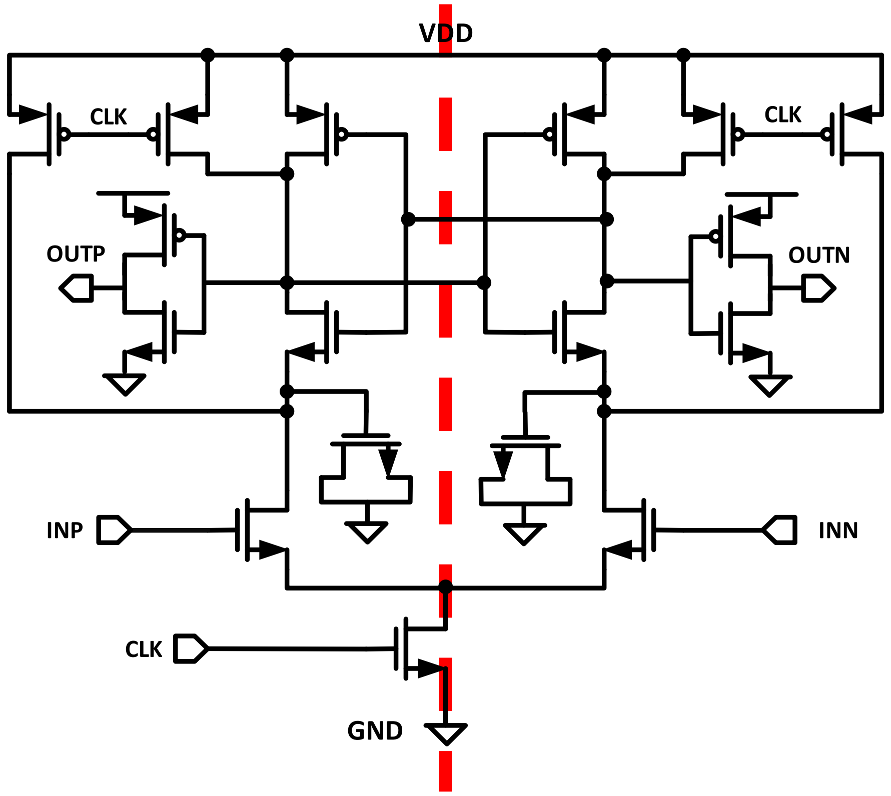
Mixed-Signal SoC

- Analog/mixed-signal IC design still heavily manual in various stages
  - Very time-consuming and error-prone

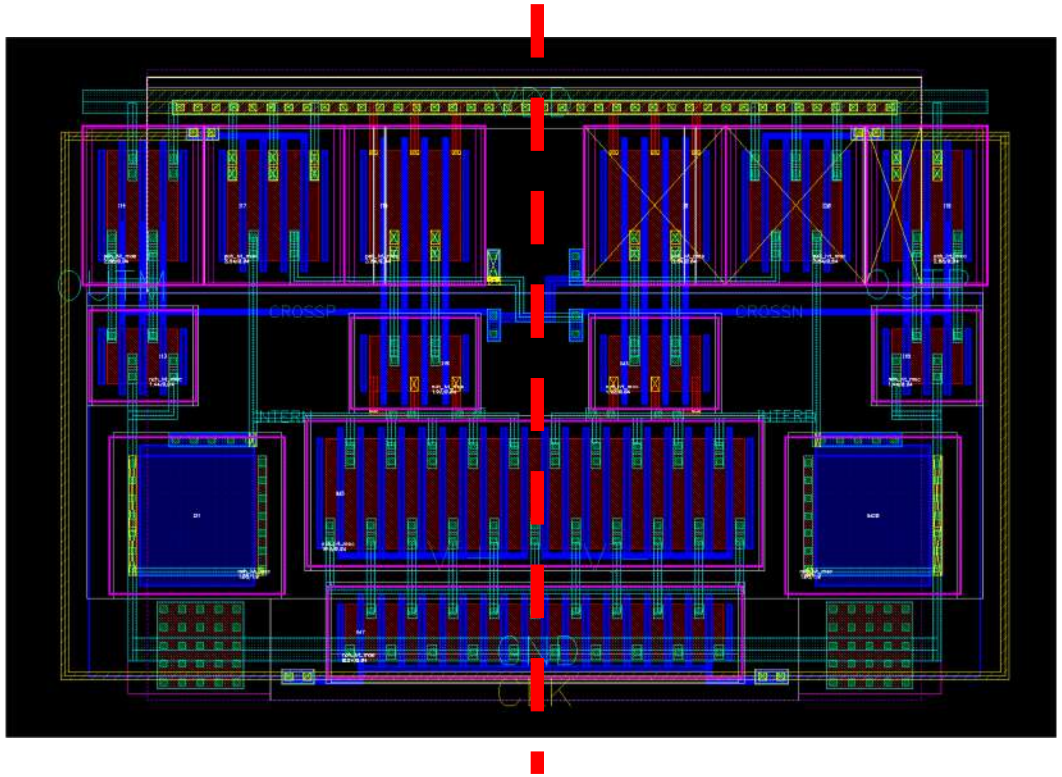
Image Sources: IBS and Dr. Handel Jones, 2012

Challenges in Analog Layout Automation

- Heavily rely on geometric constraints
  - Need to guarantee precise properties
  - Symmetry and ratio matching between devices



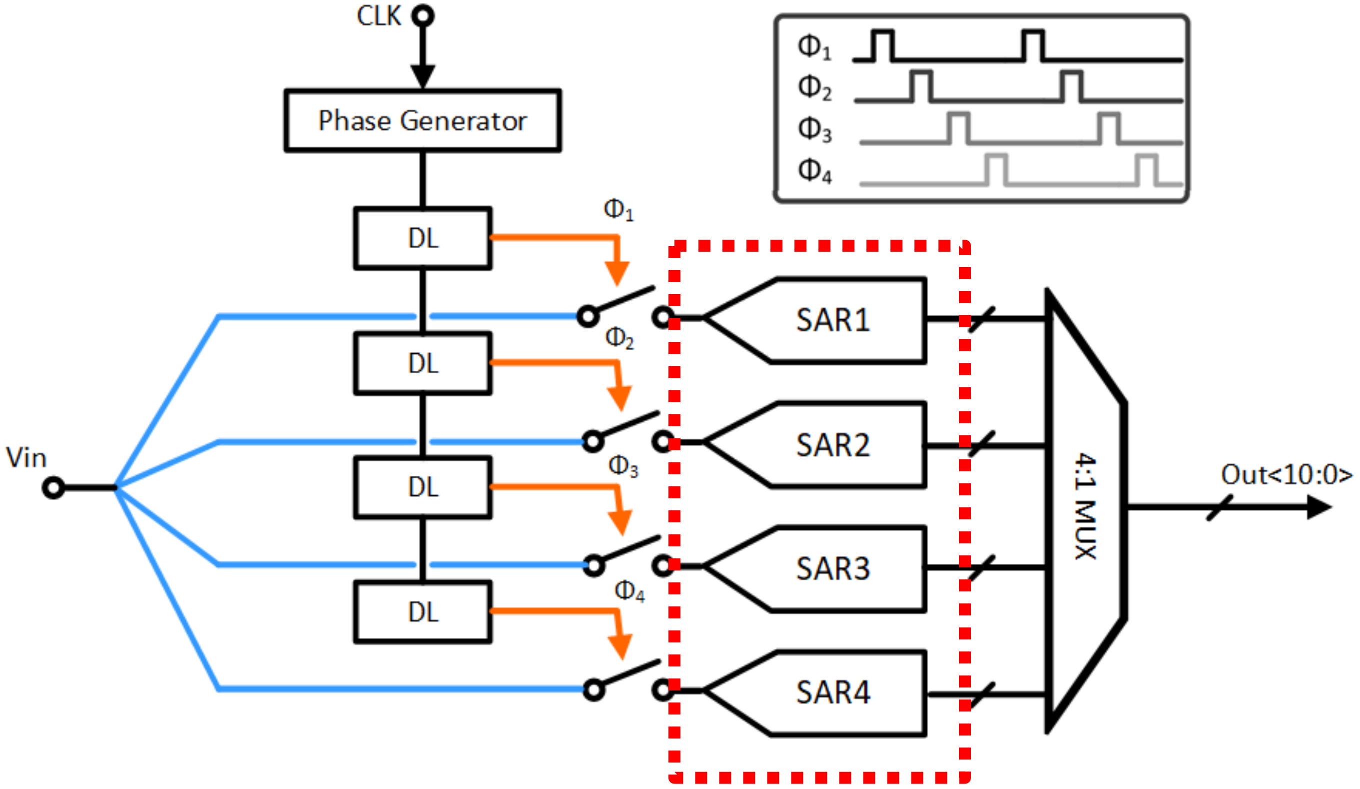
Comparator Schematic



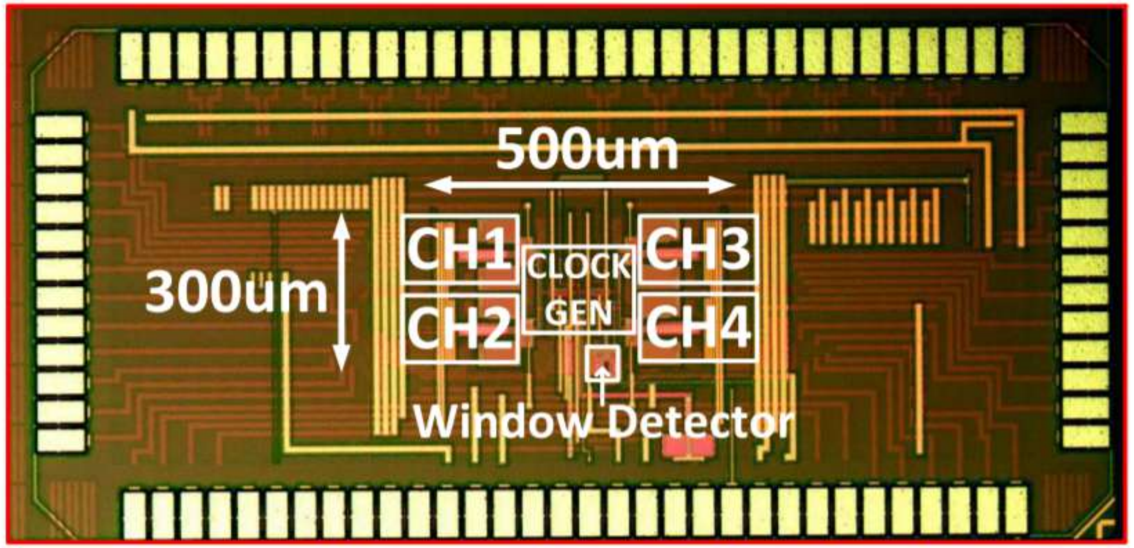
Comparator Layout

System Symmetry Constraints

- System designs require matching between building block cells



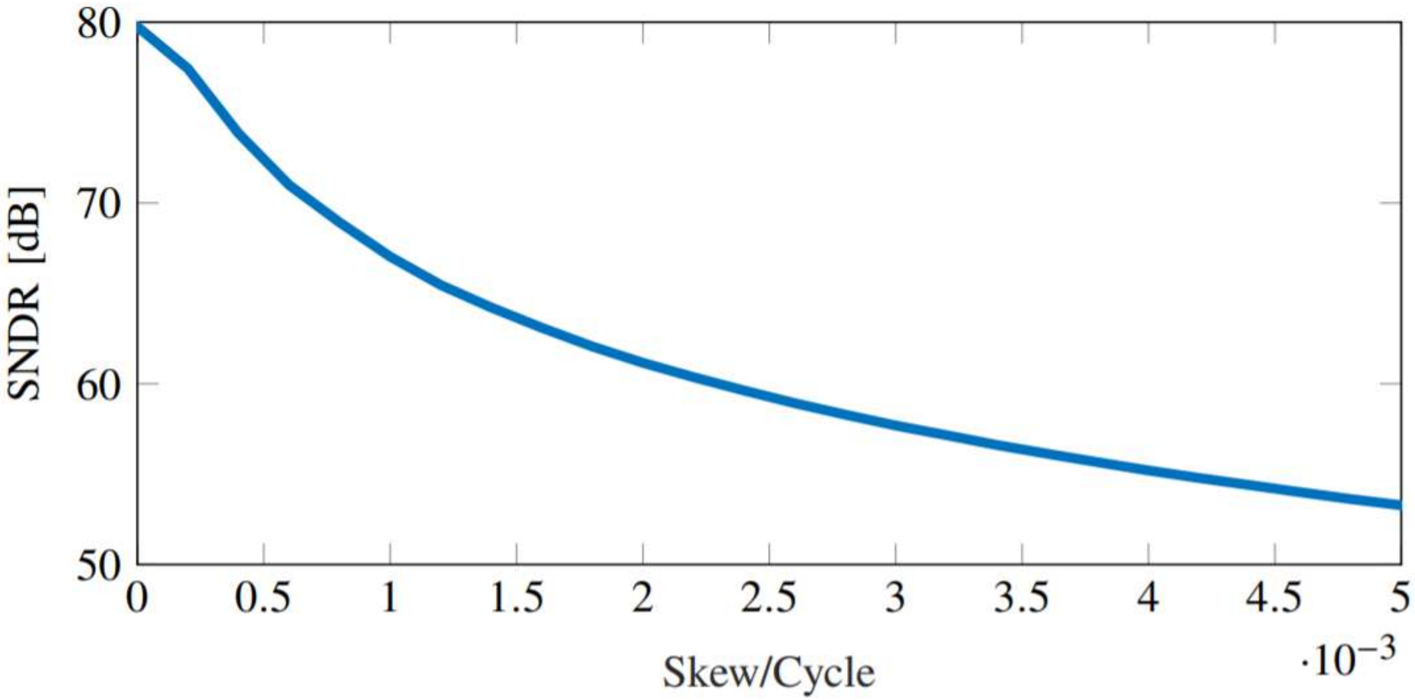
Time-Interleaved SAR ADC



Die Photo

System Symmetry Constraints

- Mismatch could cause significant system performance degradation
  - 0.1% mismatch in clock timing would result in 15dB SNDR degradation
  - Require calibration (design techniques) + careful implementation (layout)



Mismatch in clock skew between SAR channels

Prior Works: Symmetry Constraint Detection

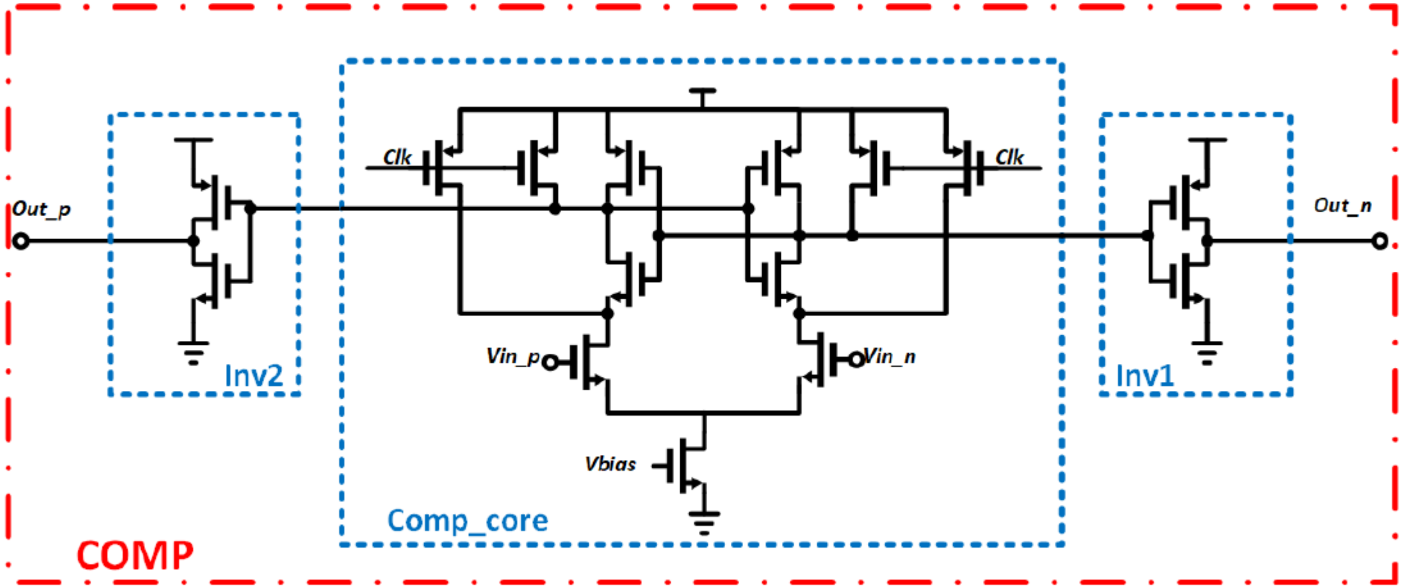
- Prior works focus on level symmetry constraints for building blocks
  - Symmetry between transistors (Mosfets and BJTs)
- Sensitivity analysis [Charbon, ICCAD’93]
  - Identify geometry constraints through electrical simulations
- Graph matching algorithms
  - Graph automorphism + signal flows [Hao, ICCCAS’04] [Zhou, ASICON’05]
  - Template circuit + subgraph isomorphism [Wu, ECCTD’15]
  - Pattern library + structural signal flow graphs [Eich, TCAD’11]

Prior Works: Symmetry Constraint Detection

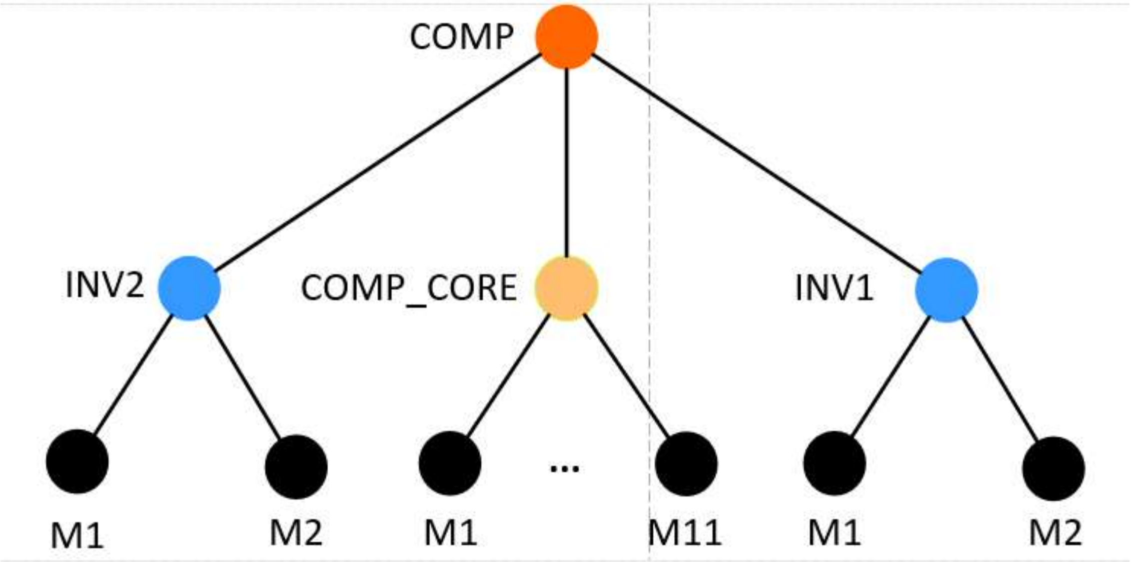
- Prior works face significant challenges when migrating to systems
  - Sensitivity analysis is unaffordable for system level designs: Transistor level spice simulations of ADCs take hours
  - Graph matching algorithms are computationally expensive: System designs normally consist over hundreds of devices
  - Difficult to generate templates/patterns for systems designs: Highly flexible and custom-designed architectures and circuits
  - Passive devices are critical in matching constraints: Capacitors and resistors

System Symmetry Constraints

- System design netlists contain hierarchy
  - Normally already well-partitioned based on functionality
  - Yield important design considerations
  - An over-simplified example:



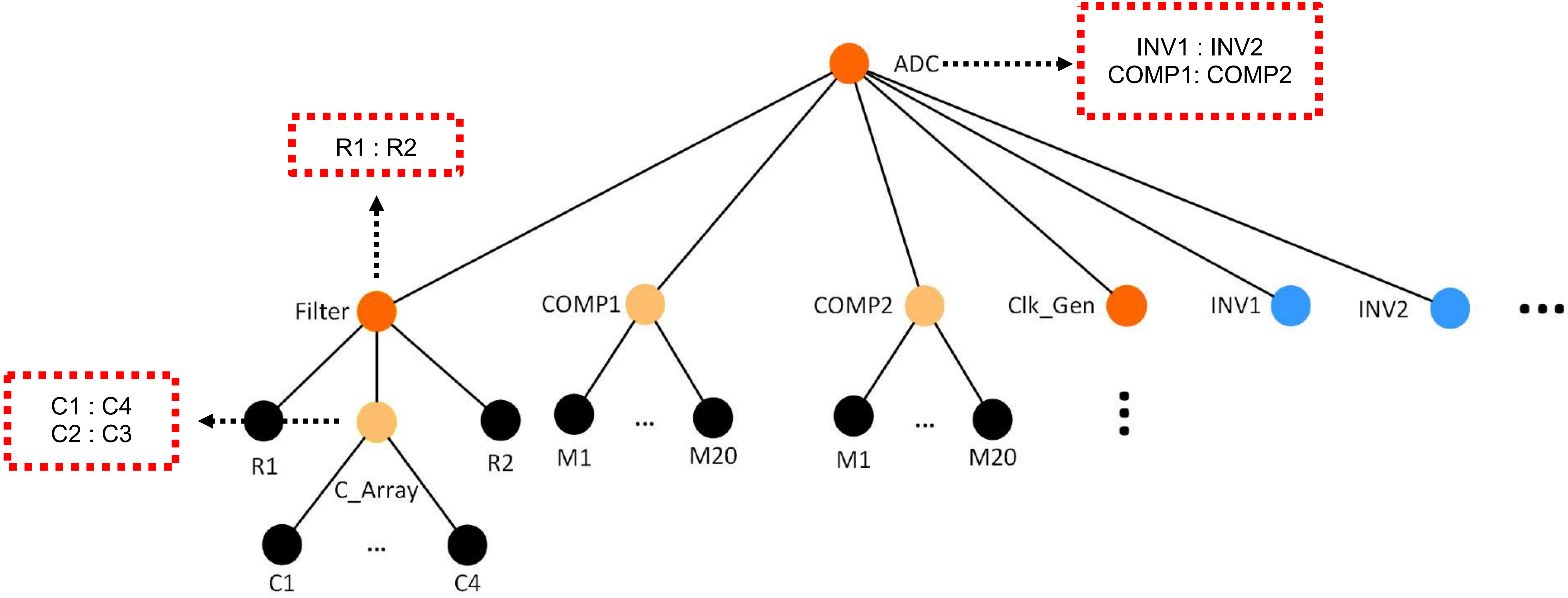
Hierarchical Netlist



Extracted Hierarchy

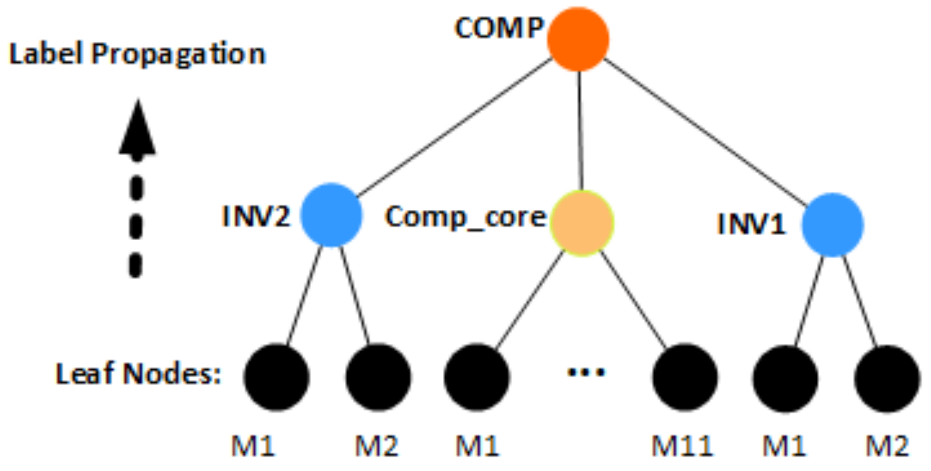
System Symmetry Constraints

- System symmetry constraints:
  - Each node in the hierarchy tree should consist constraints between its children

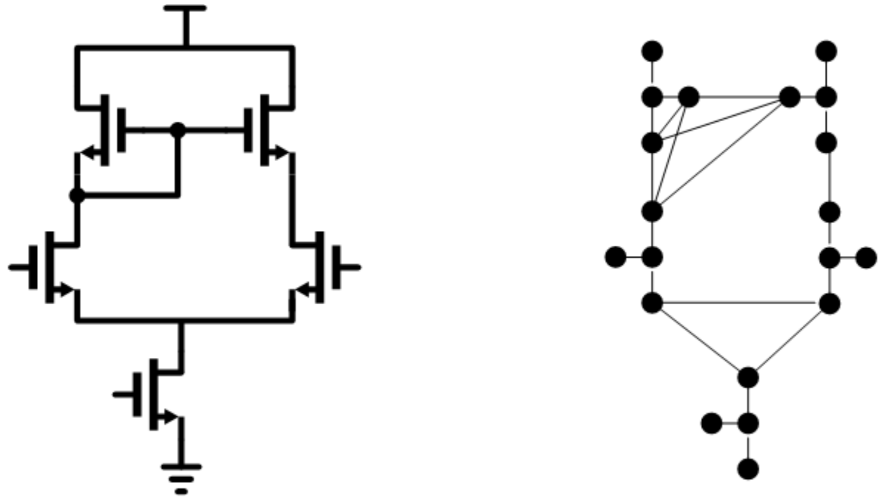


System Symmetry Constraints

- Netlist preprocessing
  - Label cells as digital or analog, propagate label through hierarchy tree
  - Generate symmetry candidates: cells with same labels
- Graph abstraction
  - Vertices: device and pins, Edges: connections
  - Easily extendable to passive devices



Label Propagation



Graph Abstraction

Overall Flow of S^{3}DET

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For any $v$ in the hierarchy graph:
    For any pair of children $(g_1, g_2)$ of $v$:
        Compare $(g_1, g_2)$ to identify symmetry constraint;
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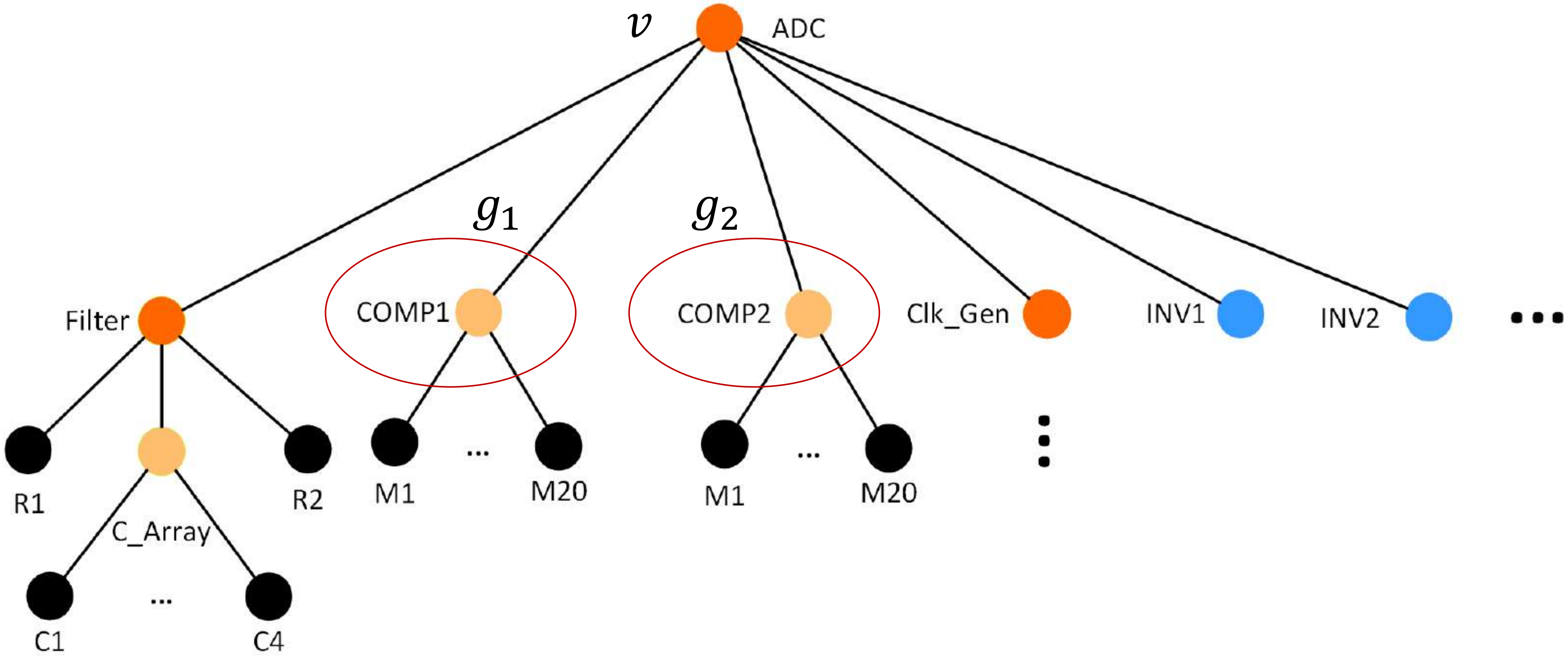
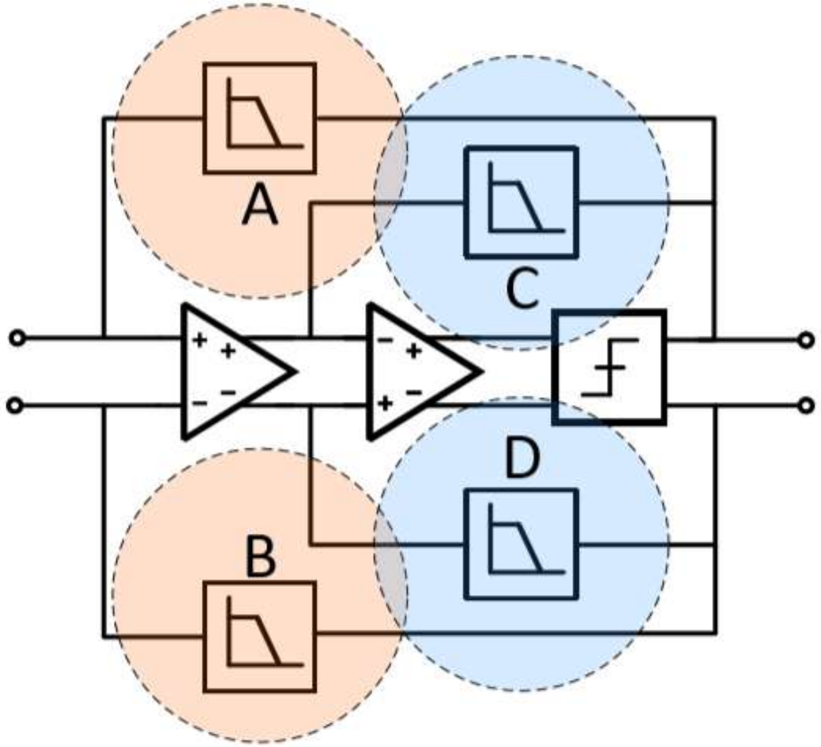


S^{3}DET

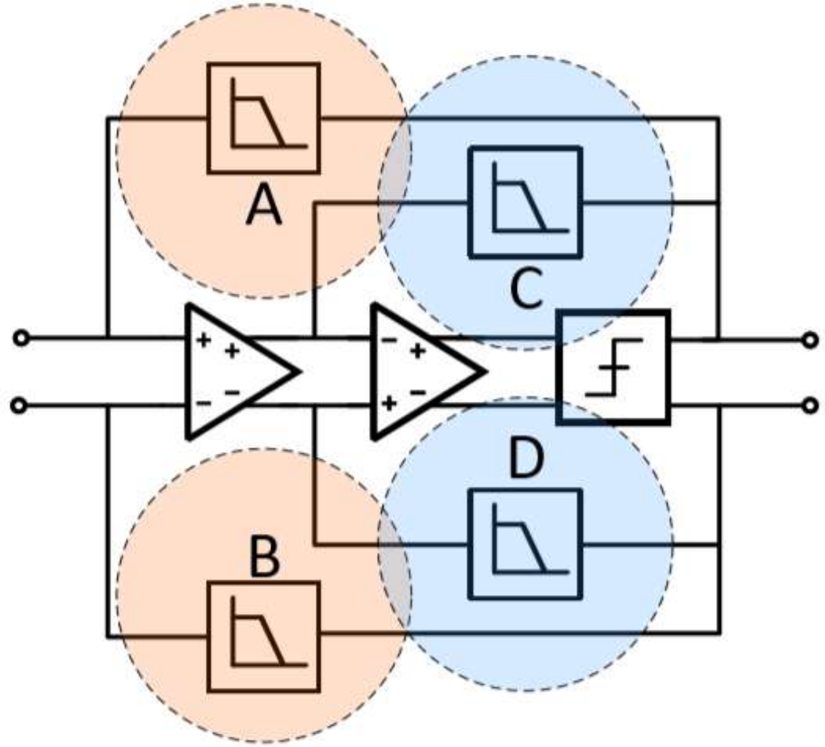
- Symmetry ambiguity
  - Only detecting subcircuits similarities does not work well in practice
  - Designers tend to reuse building blocks if possible
  - Widely used digital standard cells create lots of issues



- A, B, C, and D are the similar filters
- Only (A,B) and (C,D) need matching
- Over-constraints, such as (A,C) and (A,D) create overhead in layout parasitic or infeasible floorplans

S^{3}DET

- Resolving symmetry ambiguity
  - Extract neighboring circuit topology for each cell
  - Determine symmetry based on extracted subgraph similarity



- A, B, C, and D are the same filters
- The neighboring circuits of A is more similar compared with B, than C
- Detect symmetry based on the “context” of the circuit system

S^{3}DET

- Main Idea: Determine symmetry based on extracted subgraph similarity
  - Q: Why extract subgraphs?
  - A: Include neighboring circuit and system “context” to resolve ambiguity

  - Q: Why graph similarity?
  - A1: Graph isomorphism including neighboring circuits rare
  - A2: Graph similarity provides numeric values for comparisons

  - Problem1: We need a scalable graph similarity measurement.
  - Problem2: How large subgraphs to extract?

S^{3}DET: Graph Similarity with Spectral Analysis

- Graph similarity with spectral graph analysis
  - Graph Laplacian matrix include both degree and adjacency information
  - Its eigenvalues measure node cluster cohesiveness and have been used to approximate sparsest cuts and VLSI circuit partitions
  - We use Kolmogorov-Smirnov (K-S) statistics

$$D_n = \sup_x \left| F_{1,n}(x) - F_{2,m}(x) \right|$$

  - The p-value from the K-S test measures the eigenvalue distributions similarity, which we use as the quantitative measurement for graph similarity
  - The higher the p-value, the more similar the graphs

Gera et al., “Identifying network structure similarity using spectral graph theory”, Applied Network Science, 2018

S^{3}DET: Subgraph Extraction with Centrality

- How large subgraphs to extract?
  - Both too large and small subgraphs would result in over-constraints
  - Too large: both subgraphs are the entire system graph and always be isomorphic
  - Too small: does not include enough system context

- The subgraph size need to consider
  - The size of the subcircuits A, B
  - The proximity of the subcircuits $dist(A, B)$
  - Calculate $dist(A, B)$ with graph centers

S^3DET: Subgraph Extraction with Centrality

- Commonly used graph centrality measures
  - Jordan Center:

$$\min_{v} \max_{u \in \mathrm{V}} d(v,u)$$

  - Eigenvector Centrality:

$$\max_{v} \left(x_v = \sum_{u \in N(v)} x_u \right)$$

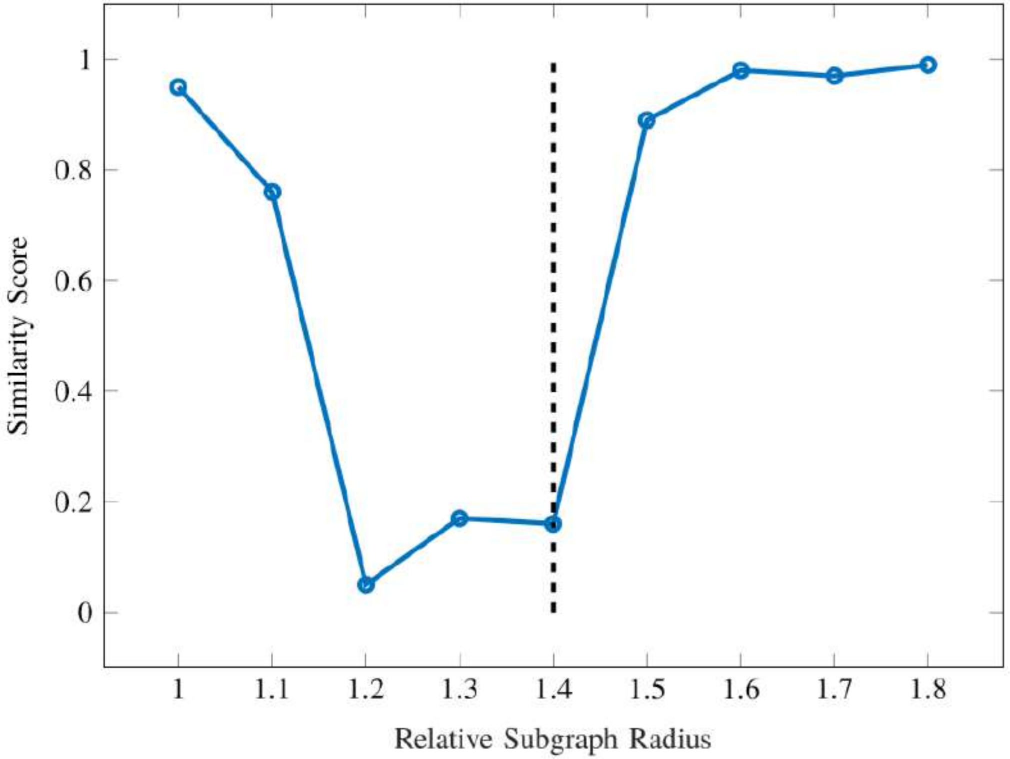
  - PageRank Center:

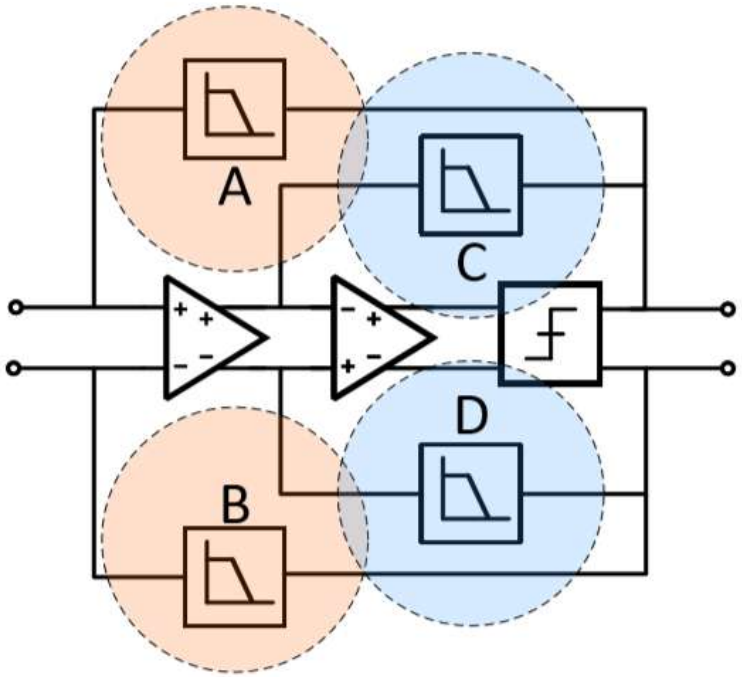
$$\max_{v} \left(PR(v) = \vartheta \sum_{u \in N(v)} \frac{PR(u)}{\deg(u)} + \frac{1-\vartheta}{|V|} \right)$$

  - We use the average of the three measures

S^{3}DET: Subgraph Extraction with Centrality

- Determining subgraph sizing:
  - Radius of subgraph = $\frac{1}{2}dist(graphA, graphC)$
  - Similarity of (A,C) is low for the proposed subgraph radius and successfully filtered this over-constraint, while a small and large subgraphs lead to over-constraint

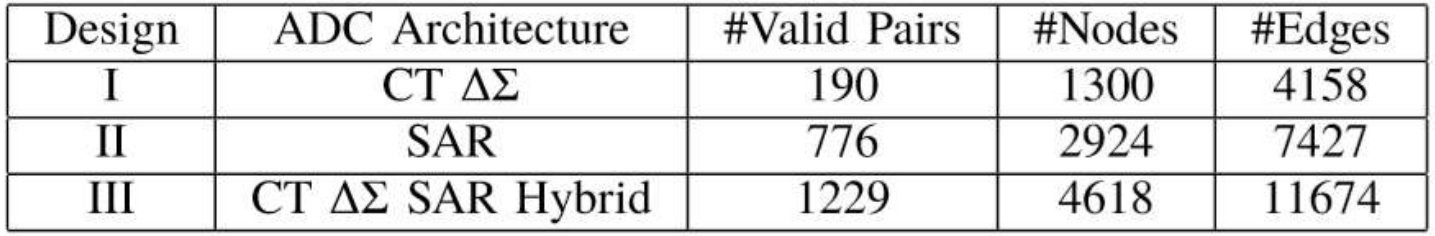




Experimental Results

- Tested S^{3}DET on 3 ADC designs and compare with labels given by designers
  - ✓ 1000+ nodes
  - ✓ 4000+ edges

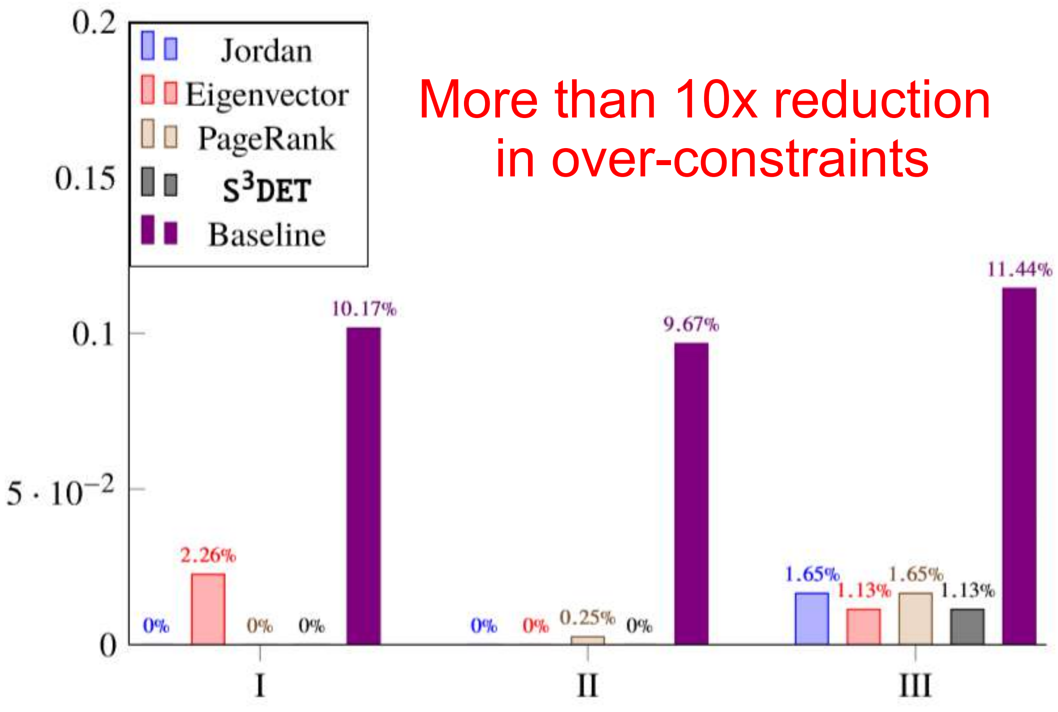
TABLE II: Statistics of ADC Designs



Design	ADC Architecture	#Valid Pairs	#Nodes	#Edges
I	CT ΔΣ	190	1300	4158
II	SAR	776	2924	7427
III	CT ΔΣ SAR Hybrid	1229	4618	11674

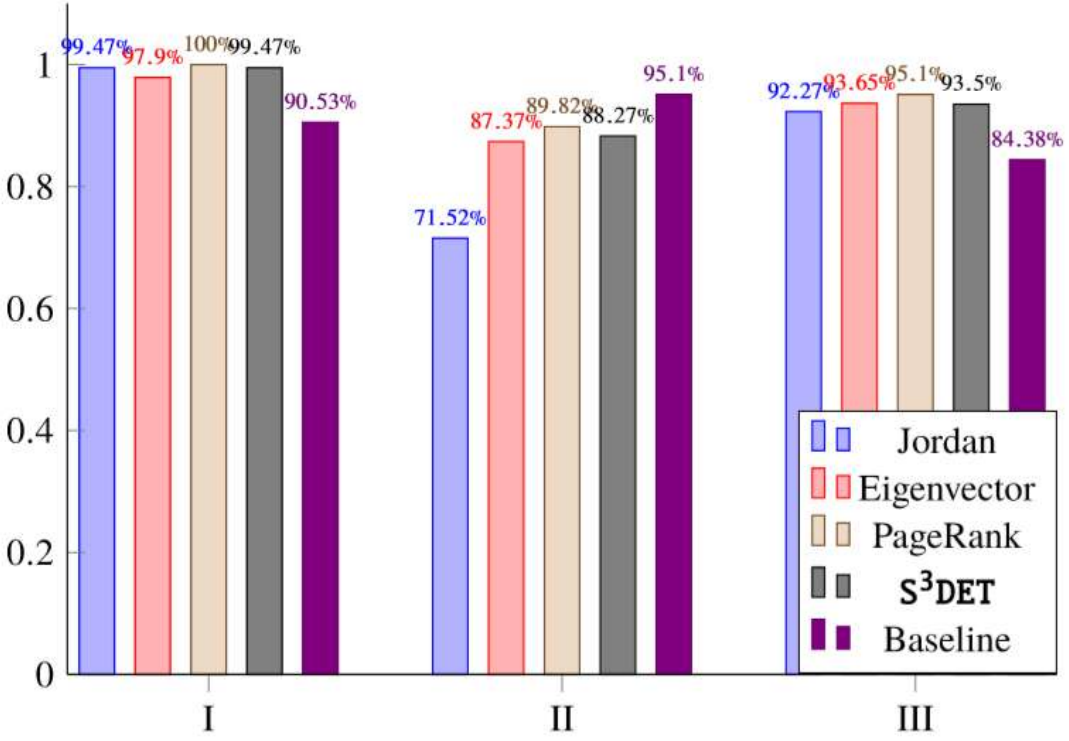
Experimental Results

- Different graph centrality have different results
- Baseline is only matching cell topology
- Overall lower false alarms (less over-constraints) with comparable accuracy and precision



More than 10x reduction in over-constraints

(c) False alarm rate



(a) Accuracy

Experimental Results

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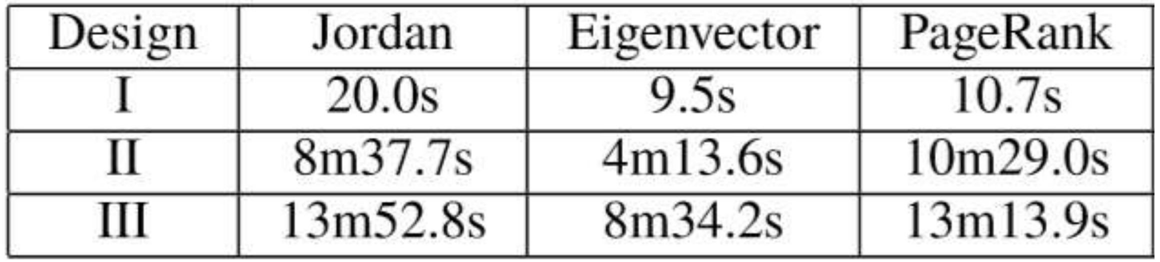


Design	Jordan	Eigenvector	PageRank
I	20.0s	9.5s	10.7s
II	8m37.7s	4m13.6s	10m29.0s
III	13m52.8s	8m34.2s	13m13.9s

Conclusions and Future Work

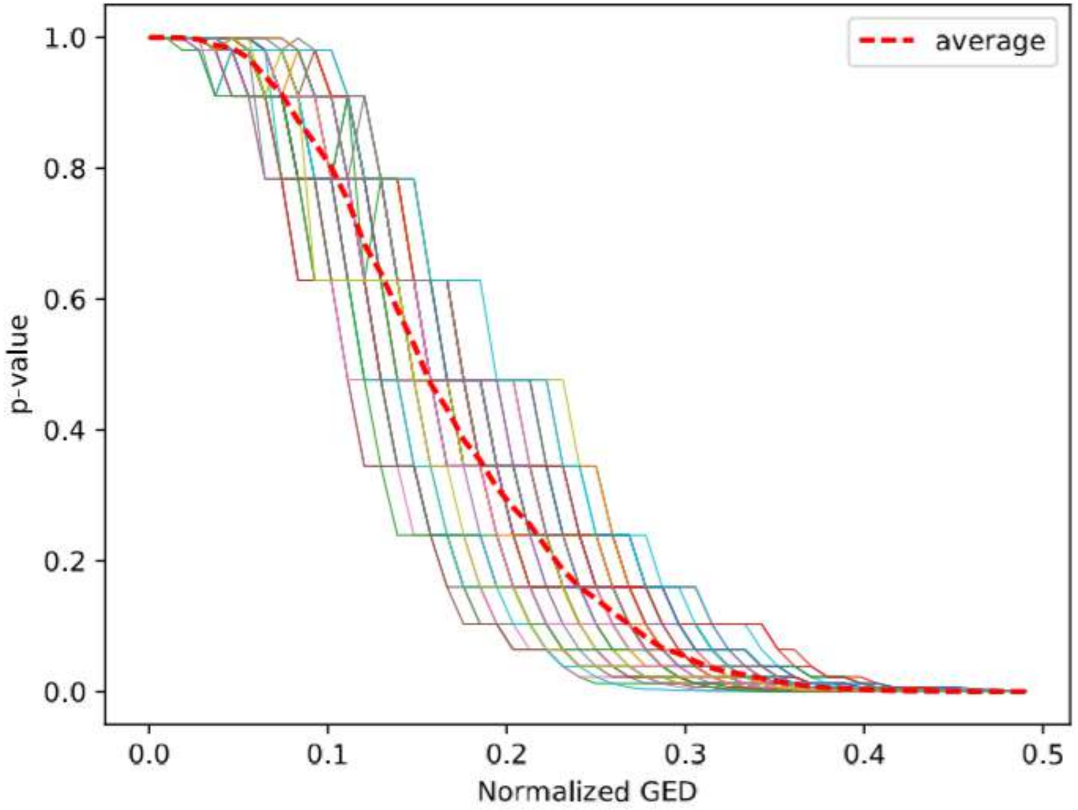
- Conclusions:
  - S^{3}DET: Method of detection system symmetry constraints
  - Subgraph extraction with graph centrality
  - Graph similarity with spectral graph analysis
  - Effectively resolve constraint ambiguity and reduce false alarms

- Future Work:
  - Extend to array-like regularity constraints
  - Fully automated layout generation for system level AMS designs

Thank You

S^{3}DET: Graph Similarity with Spectral Analysis

- Comparisons with Graph Edit Distance (GED)
  - Continuously remove edges randomly from a graph
  - Results of 50 simulations indicate strong correlations between GED and K-S p-value


average
p-value
Normalized GED