Pushing Multiple Patterning in Sub-10nm: Are We Ready?
(Invited Paper)

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ABSTRACT

Due to elongated delay of extreme ultraviolet lithography (EUVL), the semiconductor industry has been pushing the 193nm immersion lithopgrahy using multiple patterning to print critical features in 22nm/14nm technology nodes and beyond. Multiple patterning lithography (MPL) poses many new challenges to both mask design and IC physical design. The mask layout decomposition problem has been extensively studied, first on double patterning, then on triple or even quadruple patterning. Meanwhile, many studies have shown that it is very important to consider MPL implications at early physical design stages so that the overall design and manufacturing closure can be reached. In this paper, we provide a comprehensive overview on the state-of-the-art research results for MPL, from synergistic mask synthesis to physical design. We will also discuss the open problems as to pushing multiple patterning in sub-10nm.

Categories and Subject Descriptors

B.7.2 [**Hardware, Integrated Circuit**]: Design Aids

Keywords

Multiple Patterning Lithography, Layout Decomposition, Standard Cell Design, Design Technology Co-Optimization

1. INTRODUCTION

Due to the fundamental optical resolution limit, the 193nm immersion lithography can only achieve the minimum pitch (i.e., mininum width + minimum spacing) of about 80nm using single exposure. To continue the technology scaling in 22nm, 14nm, and beyond with the 193nm lithography, multiple patterning technologies have been developed to obtain finer pitches. There are two main types of multiple patterning lithography (MPL), one is based on repeated litho-etch-litho-etch (LELE) process, and the other is based on self-aligned spacer process.

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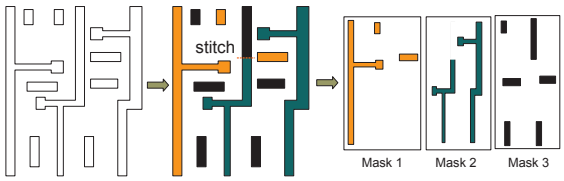

Figure 1: An example of LELELE-based triple patterning.

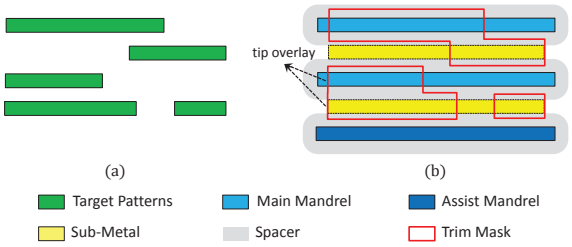

Figure 2: An example of SADP.

Fig. 1 shows an example of the triple patterning lithography with the litho-etch-litho-etch-litho-etch (LELELE) process, where the original layout is decomposed into three masks, each represented by a different color, meeting the single-exposure minimum spacing requirement. The three masks are then put together to obtain the finer pitches as specified in the original layout. It shall be noted that for LELE-type MPL, a coloring conflict sometimes can be resolved by splitting one pattern into two touching parts with different colors, resulting a stitch. However, stitch insertion may cause yield loss due to overlay error [1]. Fig. 2 shows an example of the self-aligned double patterning (SADP) with spacer-is-dielectric (SID) process to generate a tight-pitched layout.

In general, self-aligned MPL has better overlay control than LELE-based MPL, but the former typically has much more restrictions to the input layouts. Both LELE-based and spacer-based double/multiple patterning technologies have been used in fabricating critical layers which have very dense layouts, e.g., SADP has been widely used to fabricate FinFETs while LELE-based double/triple patterning has been used to print M1 layers [2–4]. In the future, MPL will still be a viable lithography solution for sub-10nm technology node, either continuing pushing 193nm lithography, e.g., using quadruple patterning [5], or used along with other

lithography techniques, such as extreme ultraviolet lithography (EUVL), electric beam lithography (EBL), and directed self-assembly (DSA) [6].

In this paper, we will provide an overview on the state-of-the-art research results for MPL, from synergistic mask synthesis to physical design. We will also discuss the open problems as to pushing multiple patterning in sub-10nm. Section 2 discusses the MPL layout decomposition problems and issues. Section 3 discusses MPL friendly standard cell (SC) design issues, including MPL compliance and pin access optimization. Section 4 discusses MPL friendly placement and routing. Section 5 concludes the paper.

2. MPL LAYOUT DECOMPOSITION

For multiple patterning lithography, one of the most fundamental problems is to decompose the layout into a specific number of masks. Then each mask should be able to manufacture under current 193nm optical lithography. If each mask is represented with one particular color, layout decomposition is equivalent to a coloring problem.

Generally speaking, when there is not enough distance between two patterns, different masks should be used to print them. It is possible that given masks are not enough to print specific features, which results in conflicts. Thus, one basic objective for layout decomposition is to avoid conflicts. In LELE-type MPL, stitch minimization is also an important target due to overlay issues, even though they can help resolve conflicts. Other objectives such as density balancing and overlay mitigation shall be considered for better printability and variations during MPL layout decomposition.

Many studies have been done on MPL layout decompositions during the stage of mask synthesis to resolve coloring conflicts, reduce stitches, balance density, or compensate overlay. In the following, we will discuss some key recent results on MPL decompositions.

2.1 LELE-Type MPL

The LELE-type MPL layout decomposition problem can be formulated into conflict graphs, in which vertices need to be colored to avoid conflicts. The problem has been proved to be NP-hard for general layouts [7]. To solve the problem with reasonable runtime for general layouts, several graph simplification techniques have been proposed. Yu et al. [8] proposed three techniques for TPL decomposition, i.e. connected components computation, removing vertices with degree less than three, and 2-edge-connected component computation. Fang et al. [9] further gave two techniques called *2-connected component computation* and *3-edge-connected component computation*. A layout can be even divided into small clusters for further speedup [10].

To solve the coloring problem, both optimal algorithms and approximation algorithms have been proposed. The first ILP formulation and a semidefinite programming (SDP) based approximation algorithm are provided by [8]. Then several heuristic based methods are proposed [9–11]. Ghaida et al. [12] tried some methods to reuse the DPL decomposer for TPL.

The SDP approximation algorithm proposed by Yu et al. [8] can be extended to handle any k-patterning problem. It is able to achieve tradeoffs between quality and efficiency compared with ILP formulation. The basic idea is to formulate a vector programming problem by introducing a set of unit vectors. For example, in quadruple patterning, four vectors are introduced in the SDP formulation from [5]: $(0,0,1)$, $(0,\frac{2\sqrt{2}}{3},-\frac{1}{3})$, $(\frac{\sqrt{6}}{3},-\frac{\sqrt{2}}{3},-\frac{1}{3})$ and $(-\frac{\sqrt{6}}{3},-\frac{\sqrt{2}}{3},-\frac{1}{3})$ to represent four different masks (see Fig. 3). If two vectors have the same color, $\vec{v_i}\cdot\vec{v_j}=1$; otherwise, $\vec{v_i}\cdot\vec{v_j}=-\frac{1}{3}$.

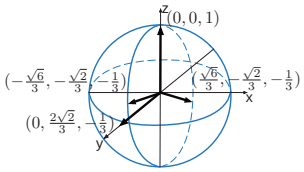

Figure 3: Vector based color representations.

The generalized SDP formulation for k-patterning layout decomposition where $k \geq 4$ is shown as follows [5],

$$\min \sum_{e_{ij}\in CE}(\vec{y_i}\cdot\vec{y_j}+\frac{1}{k-1})+\alpha\sum_{e_{ij}\in SE}(1-\vec{y_i}\cdot\vec{y_j}) \quad (1a)$$

$$\text{s.t.} \quad \vec{y_i}\cdot\vec{y_i}=1, \quad \forall i\in V \quad (1b)$$

$$\vec{y_i}\cdot\vec{y_j}\geq -\frac{1}{k-1}, \quad \forall e_{ij}\in CE \quad (1c)$$

where vector $\vec{y_i}$ is the continuous relaxation of discrete vector $\vec{v_i}$. The corresponding discrete vector program is relaxed to a continuous SDP problem. With an appropriate rounding scheme, the colors for most vertices can be determined.

For some special layout structures, polynomial time exact algorithms exist for layout decomposition. Cork et al. [13] studied the scalability of different coloring algorithms with various contact patterns. For a standard cell based row-structure layout, Tian et al. [14] proposed a polynomial time algorithm to find an optimal solution. Further study has been done for constrained pattern assignment where the color solutions for the same type of standard cells are required to be the same [15]. By reducing the graph size and parallelization, decomposers are capable of computing solutions in even shorter time [16, 17].

While it is true that providing a coloring solution is substantial to layout decomposition, the importance of colorability check should be highlighted as well. Fast colorability checkers that are able to report the positions of unresolved conflicts are urgently desired. If the unresolved conflicts can be accurately located, they can be fixed either manually or automatically during the post-layout stages.

There are also some studies on MPL layout decomposition considering balanced density control [18, 19]. In terms of mitigating the overlay induced timing variations, [20] proposed an simple yet effective color interleaving technique for double patterning lithography. However, there are no such studies yet on triple patterning layout decomposition and beyond. Another concern lies in the correlation between stitches and actual yield loss. The impact of stitches on yield varies from pattern to pattern. Some stitches are critical and very likely to result in hotspots, while the others may not. Therefore, further efforts are needed to distinguish stitches during decomposition stage. It is also very meaningful to detect hotspot features and even take OPC friendliness or process variations into consideration.

2.2 Spacer-Type MPL

Spacer-type MPL typically refers to SADP and SAQP. Both techniques have very restrictive constraints in width and spacing rules. The insertion of stitch is not allowed

either. The discrepancy between the trim mask patterns and the original layouts further results in the complexity of SADP layout decomposition.

ILP was formulated [21,22] to solve this problem. The formulation of ILP is flexible so it is able to integrate other objectives like lithography hotspots. But runtime is a challenge for this approach. Ban et al. [23] proposed an SADP layout decomposition framework for 2D layout structures. The problem is formulated into a 2-coloring problem, as shown in Fig. 4. The blue color denotes the patterns manufactured by the mandrel mask, while the red color represents the patterns for the trim mask. In 2D layouts, it is possible to have inherent conflicts such as B and C. Once such kind of conflicts are detected, original core masks should be merged smartly so that undesired patterns can be trimmed out by the trim mask. After the removal of all conflicts, layout decomposition can be solved with 2-coloring techniques. Recently, Xiao et al. [24] showed that 2-colorability is necessary to achieve an SADP decomposition solution without any overlay. They proposed a new graph formulation and solved a 2SAT problem in polynomial time, which guarantees to return a valid solution as long as one exists. Then merging techniques were employed to explore larger solution spaces for standard cell row-structure layout [25].

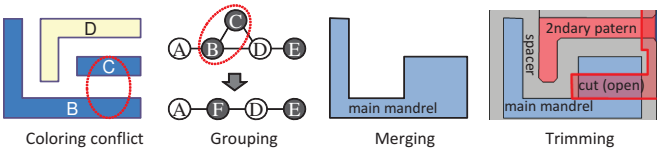

Figure 4: Grouping and merging coloring for spacer-based multiple patterning [23].

The overlay issue for spacer-type of MPL can be mitigated by various approaches mentioned previously. It cannot be completely avoided due to the misalignment at the trim mask. Thus, overlay reduction and hotspot detection are still important issues for layout decomposition. Furthermore, while similar principles in SADP can be applied to SAQP, there are very limited studies on self-aligned multiple pattern (SAMP) and beyond.

2.3 Decomposition for Hybrid Lithography

In order to further push the lithography resolution, hybrid methods have been proposed [26, 27]. Traditional 193nm optical lithography is applied together with high-resolution lithography approaches. The flow of hybrid lithography consists of two stages. In the first stage, conventional optical lithography or SADP is used to print base features. In the second stage, some redundant areas are cut by high-resolution lithography methods, like EUVL or EBL. While it is true that better image quality can be achieved by hybrid approaches, there will be inevitable increase in the manufacturing cost. It is also necessary to figure out the way to generate features under the new approaches. Some studies have been done to combine SADP and EBL [27, 28] and then an extension to 2D layout design has been proposed [29]. Recently, Yang et al. [30] proposed a random-initialized local search method to combine MPL and EBL when considering stitch minimization and EBL throughput simultaneously.

3. MPL STANDARD CELL DESIGN ISSUES

For the standard cell (SC) designers, it is important to provide a robust library that can be applied in any design implementation. In sub-10nm, middle-of-line (MOL) layers routinely introduce multi-cell interactions under MPL constraints [31]. To improve the library-level MPL robustness, efficient multi-cell evaluation over MPL constraints is critical to provide quick feedback to the designers for incremental SC layout modification/migrations. Moreover, the SC input/output (I/O) pins are difficult to access with limited number of routing tracks under complex MPL constraints. In this section we present several techniques, including SC pre-coloring, library robustness evaluation and pin access optimization, to enable SC compliance under MPL constraints.

3.1 Standard Cell Pre-Coloring

To design a library compatible with MPL constraints, designers need to ensure that the layout of each cell is MPL-friendly. If coloring conflicts are detected, further layout modifications/migrations are needed [32,33]. Then, SC pre-coloring is to perform layout decomposition up front, and embed the coloring solutions for each type of cell into the library [33,34]. During later design stages, the coloring solution for each cell instance can be quickly achieved by querying the cell library.

Figure 5: (a) Sample layout and the corresponding conflict graph. (b) Simplified conflict graph. (c) Pre-coloring solutions for triple patterning [33].

For the pre-coloring of each type of cell, we construct a conflict graph to represent the topological relationship among layout patterns. Fig. 5 (a) shows a sample layout and its corresponding conflict graph for triple patterning. In particular, only the color assignment for boundary features will be enumerated and the simplified conflict graph is shown in Fig. 5(b). A set of graph coloring solutions are computed for the color assignment of all patterns [33, 34]. Note that the coloring solution of a single cell may not be unique. To allow the maximum placement flexibility, all legal coloring candidates are enumerated and embedded into the cell library (see Fig. 5(c)).

3.2 Library Robustness Evaluation

The SC pre-coloring targets at MP-friendly layout design and a set of legal coloring solutions for each type of SC in isolation. However, for practical designs, various SC instances will be placed close to each other and the MPL constraints introduce interactions among them [31, 33]. The 3-cell interaction examples for triple and quadruple patterning are shown in Fig. 6(a) and Fig. 6(b), respectively. At the library design level, SC designers target at improving the inter-cell compatibility for all combinations of cells, regardless of what kind of placement [2]. With MPL applied to multiple layers with small feature sizes [2,3], it is difficult to

guarantee that any combination of SC's is compatible with MPL coloring constraints. However, a robust library should minimize the number illegal SC's combinations that lead to MPL coloring violations. During library development stage, an efficient framework is necessary to quickly achieve the number of illegal cell combinations and associated standard cell types for the purpose of incremental SC layout modifications/migrations,. The library evaluation framework in [31] focused on the MOL layer that routinely leads to interactions across SC boundaries and aimed at quickly providing the illegal cell combinations and associated SC's to the designers. In the future, it is worthwhile to extend this framework to other MPL layers, such as Metal-1.

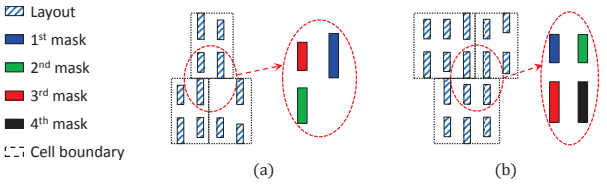

Figure 6: 3-cell interactions. (a) Triple patterning. (b) Quadruple patterning [31].

3.3 Pin Access Optimization

With fixed number of routing tracks for SC design, the access points for each I/O pin are limited, which makes the SC I/O pin access particularly challenging under extra MPL constraints. One way the SC designers can improve the SC pin accessibility is to intelligently design the I/O pins, which maximizes the number of access hit points for each I/O pin of the SC's [2, 3]. However, the complicated MPL constraints introduce interactions among neighboring access points of different I/O pins of the SC's. For modern SC designs, Metal-1 layer is primarily used for the I/O pin design and intra-cell connections for the SC layout. This makes Metal-2 layer essential for local I/O pin access of the SC's. SADP is a competitive lithography candidate for the lower metal layers including Metal-2 for pin access. For SADP-based Metal-2 wires, legal line-end positions depend on both via placement and neighboring wire placement. As shown in Fig. 7, the line-end extensions beyond the via positions are necessary to retrieve valid Metal-2 wires for one pin access candidate. In general, pin access and SC layout co-optimization shall search for all legal intra-cell pin access solutions with line-end extension techniques, to provide maximized pin access flexibility for the detailed routing stage.

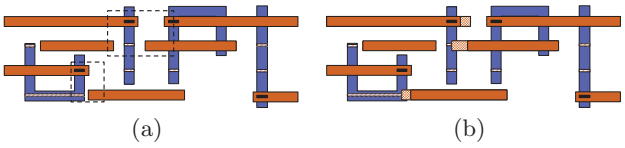

Figure 7: Pin access optimization for one pin access candidate. (a) Design rule violations. (b) Optimized Metal-2 wires [35].

3.4 Future Cell Architecture

For sub-10nm SC design, MPL is expected to be widely used across various device layers. Unidirectional layout will be favorable since the bidirectional patterns are not compatible with high-order frequency multiplication, such as SAQP. A systematic library regularity design and robustness evaluation framework will be crucial to provide good starting point of SC design and quick feedback on the quality evaluation under MPL constraints [36]. Additional metal layers for intra-cell routing, such as M0 or Mint [2, 3], may be introduced to reduce the usage of Metal-2 wires for SC design, which is crucial for better local pin access during the routing stage. However, the interactions among access points of various I/O pins are expected to be more significant under complicated MPL constraints, which makes the SC level pin access design/optimization particularly important.

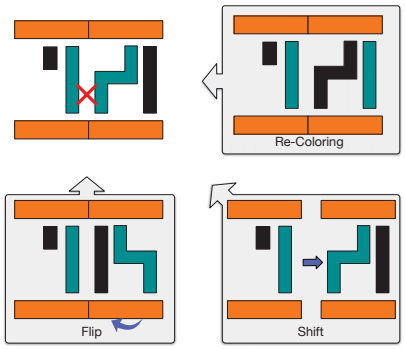

Figure 8: Three techniques to remove MPL conflicts during placement.

4. MPL FRIENDLY PLACE AND ROUTE

Since redesigning indecomposable patterns in the final layout requires high engineering efforts, layout decomposition itself may be too late and MP-friendly layout designs in the early physical design stages including placement and routing, becomes urgent and pivotal. In sub-10nm technology node, it is difficult to allow arbitrary SC's combinations that are compatible with each other under MPL constraints [31, 33], which makes the extra placement-level efforts inevitable to resolve inter-cell coloring conflicts. To systematically achieve legal routing results, it is important to incorporate MP-specific constraints into the routing stage.

4.1 MPL aware Placement

In the SC pre-coloring stage, a set of coloring solutions have been pre-computed for each type of cells in the library. One single type of cell might be applied multiple times for practical designs and SC instances are placed next to each other. Although the coloring conflicts have been resolved within each cell instance during library design stage, extra coloring conflicts may be introduced when cells are placed next to each other as shown in Fig. 8, which brings the necessity of MP-aware placement.

Several studies have been shown to resolve the inter-cell coloring conflicts during the placement stage. Gupta et al. presented the timing and yield aware color assignment for SC's for double patterning lithography [37]. Gao et al. proposed the placement legalization based on SC pre-coloring for SADP [38]. Given pre-coloring solutions for SC's, Agarwal et al. proposed a dynamic programming algorithm to resolve coloring conflicts for general MPL [39]. In particular, there has been several studies focusing on the triple

patterning aware placement problem. Yu et al. [33] developed three techniques, including cell re-coloring, cell flipping and cell shifting, as illustrated in Fig. 8, to resolve the conflicts between cells for triple patterning. In particular, the cell re-coloring is obtained by selecting a compatible coloring solution for the target cell by querying the pre-computed coloring solutions. By incorporating the techniques to resolve inter-cell conflicts, the triple patterning aware ordered single row placement can be formulated as a shortest path problem and solved optimally. Tian et al. further considered the constrained pattern assignment for the same type of SC and a weighted partial MAX SAT approach was proposed [40]. Kuang et al. presented both global and local moving techniques and better placement quality was reported [41]. Lin et al. demonstrated the placement refinement problem for triple patterning under constrained pattern assignment is NP-complete and a mixed integer linear programming approach along with efficient heuristics was presented [42]. However, most existing studies focus on the single-row placement with coloring constraints. For sub-10nm, some device layers, such as MOL layers, routinely introduce inter-row interactions, which brings the necessity of placement-level efforts to resolve the coloring conflicts across adjacent placement rows. We expect to see more research efforts along this direction in the placement level.

4.2 MPL aware Routing

In sub-10nm technology node, the high routing density and small pitches of the routing patterns bring the need of MPL for the lower metal layers, such as Metal-2 and Metal-3. MP-aware routing will be crucial to obtain more flexibility and better quality for the routing results.

Different from double patterning, detecting triple patterning or the general MPL coloring conflicts during routing will be more sophisticated due to the higher complexity of conflict graph and color assignment. Ma et al. proposed an expanded routing grid model to systematically deal with triple patterning coloring constraints during the routing stage [43]. Another general MPL coloring technique during routing stage was proposed by Lin et al. [44]. A special data structure, token graph-embedded conflict graph (TECG) consisting token graph (TG) and conflict graph (CG), is proposed to facilitate coloring conflict detection. To reduce the yield loss from stitches, a conflict graph precoloring approach was proposed by Hsu et al. [45].

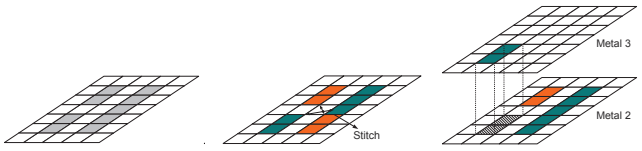

Figure 9: Prevent conflicts by prescribed layer assignment. (a) Target layout. (b) Conflicts (shown as arrows) remains even with stitch insertion. (c) Conflict removed by layer assignment [34].

Furthermore, due to better overlay and line edge roughness control compared to LELE-type MPL, SADP/SAQP are treated as competitive lithography candidates for the lower routing layers with tight pitches in sub-10nm technology nodes. Mirsaeedi et al. [46] presented an early work on the SADP-friendly detailed routing. To effectively resolve coloring conflicts during SADP-aware routing, Gao et al. [38] developed corresponding *layer assignment* technique, which can be performed to separate conflicting patterns into different routing layers (see Fig. 9). By integrating the prescribed routing patterns together with the routing cost, it is possible to simultaneously perform multi-layer routing and layout decomposition in a correct-by-construction manner for SADP [38]. Kodama et al. [47] proposed novel grid coloring strategies for both SADP and SAQP with hotspot reduction in the routing patterns. A specialized graph model for sidewall is dielectric type of SADP aware routing was proposed by Du et al. [48] to achieve legal routes while minimizing the SM-jog penalties. Liu et al. [49] proposed a novel overlay constraint graph to guide SADP-aware routing while minimizing the amount of overlay. A full chip wire planning and SAQP-aware routing method was further presented by Fang et al. [50]. To address the handshake between the SC level pin access and detailed routing stage, Xu et al. proposed a holistic pin access planning and regular routing framework for SADP to improve the overall detailed routability [51]. In sub-10nm, the tight pitches of lower metal layers brings the need of MPL for the corresponding via layers. Complicated neighboring interactions from MPL constraints on the via layer could introduce additional difficulties on SC local pin access and detailed routing stage. We expect to see more research efforts on resolving MPL constraints for multiple via and metal layers simultaneously to achieve high-quality MPL friendly routing results.

5. CONCLUSION

In the last few years, we have seen double patterning lithography from concept to deployment to produce the most advanced IC chips, e.g., in 22nm and 14nm technology nodes. Due to the delay of EUVL, triple patterning is now being adopted for the 14nm/10nm nodes, and quadruple patterning or beyond is under serious consideration for the 7nm node. This paper has summarized some key recent results for MPL, from mask design to physical design. While many research studies have been performed on MPL related mask and physical design, there are still many open research problems as pointed out in the paper. Ultimately how much further to push MPL really depends on the cost, overlay control, and the cost-effectiveness of extreme scaling. Even with the final adotpion of EUVL or other emerging lithography, the paradigm of multi-patterning is still very interesting as it can be used together with these emerging lithography technologies.

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