Minsik Cho

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Research Interest

- Design-for-Manufacturability/Reliability (DFM/DFR) for Nanometer IC Design.
  - Holistic Uncertainty (Manufacturability+Reliability) Closure.
  - DFM/DFR with Design-for-Testability/Diagnosis (DFT/DFD).
  - Design and Process Integration for Nanolithography.
- Design Closure on New Computing Platforms (multi/many-core, coprocessor, and etc.).
- CAD for Analog/Mixed-signal design.
- Design Automation for Emerging Technologies (nano/bio/MEMS/NEMS).

Teaching Interest

Undergraduate: VLSI design, logic design, computer architecture, operating system, programming, algorithms and data structures, computer networks.

Graduate: Advanced VLSI design and CAD, VLSI physical design, VLSI manufacturability/reliability optimization, Advanced algorithms and combinatorial optimization.

Education

Ph.D. in Electrical and Computer Engineering, expected in May 2008
Advisor: Dr. David Z. Pan
Thesis: Manufacturability and Reliability for Nanometer VLSI Physical Synthesis
University of Texas at Austin, Austin, TX

M.S. in Electrical and Computer Engineering, May 2004
University of Wisconsin Madison, Madison, WI

B.S. in Electrical Engineering, February 1999
Seoul National University, Seoul, Korea

Professional Experience

Summer Internship — **IBM T. J. Watson Research**
Logic and Physical Synthesis Dept. — **Yorktown, NY**
May 2007 – Aug 2007

I implemented a logic cluster aware physical partitioning for parallel physical synthesis and timing closure in IBM PPDS (Parallel Placement-Driven Synthesis) environment, targeting for multi/many-core architectures. It was featured with a systematic approach for gate weight computation and a min-cost network flow algorithm.

Summer Internship — **IBM T. J. Watson Research**
Logic and Physical Synthesis Dept. — **Yorktown, NY**
Jun 2006 – Aug 2006

I implemented a prototype Design-for-Manufacturability (DFM) router in IBM PDS (Placement-Driven Synthesis) environment. It was featured with simultaneous layer assignment, congestion awareness, and CMP/topography variation reduction. Compared with an IBM industrial router, my approach showed very encouraging results.

Summer Internship **Intel Austin Design Center**
Mobile Chipset Group **Austin, TX**
May 2005 – Aug 2005

I was in charge of establishing a power model for the latest Intel mobile chipset, ICH7. At the end of internship, I successfully came up with a power model which makes use of architectural activities to estimate the power consumption on runtime for thermal throttling.

Graduate Research Assistant **University of Texas at Austin**
UT Design Automation Lab **Austin, TX**
Sep 2004 – Present

I have researched on VLSI CAD algorithms under the supervision of Prof. David Z. Pan. My main research has focused VLSI physical synthesis for manufacturability /reliability (DFM/DFR) and high performance global routing, but also covered biochip design automation, CAD algorithms on multi/many-core architectures, and VLSI testing.

Graduate Teaching Assistant **University of Texas at Austin**
System on Chip Design **Austin, TX**
Jan 2005 – Dec 2005

I was a TA for Prof. Jacob A. Abraham's EE 382V: System-on-a-Chip Design. As this class was first introduced in 2004 Fall, I developed the main course labs and project where a Software Defined Radio System, DRM (Digital Radio Mondiale) was implemented using an ARM based platform design methodology.

Graduate Project Assistant **University of Wisconsin Madison**
Smith M. Lloyd Group (Chemistry Dept.) **Madison, WI**
Nov 2002 – May 2004

I worked on a project of DNA computing where my main task was to design a set of DNA sequences such that mishybridization between two different sequences can be minimized based thermodynamic stability analysis. I solved a set of SAT problems using DNA computing to demonstrate its potential and scalability.

Senior Software Engineer **CNG Soft Co.**
Seoul, Korea
Apr 2002 – Aug 2002

I was a project manager to design and develop a TCP/IP based real-time audio, video capturing system, based on MPEG4 and Speex/Ogg.

Software Engineer **MC Global Co.**
Seoul, Korea
Feb 1999 – Apr 2002

I designed and developed a part of a multicast based real-time video conferencing system which is compatible with H.323/SIP VoIP protocol.

Awards/Honors/News Coverage

SRC Inventor Recognition Award, Semiconductor Research Corporation, 2008

IBM Ph.D. Scholarship in recognition of academic excellence, IBM Corporation, 2007-2008

IEEE/CEDA Award for BoxRouter 2.0 open source, 2007

ACM/SIGDA Awards in the routing contest during ACM International Symposium on Physical Design (ISPD), 2007 - 2nd Place (3D) and 3rd Place (2D), and completed the most number of circuits (12 out of 16 circuits) among over 12 teams from US and Asia, including entries from industry

EE Times Coverage, March 22, 2007, "IC routing contest boosts CAD research,"

http://www.eetimes.com/news/design/showArticle.jhtml?articleID=198500084

EE Times Coverage, June 19, 2006, "Chip designers feel the heat - Accurate thermal analysis cools the effects of sub-90-nm design,"
http://www.eetimes.com/news/design/showArticle.jhtml?articleID=189400781

Best Paper Award Nomination, ACM/IEEE Design Automation Conference (DAC), 2006 (12 nominations out of 865 submissions)

Best Paper Award Nomination, ACM/IEEE Asian and South Pacific Design Automation Conference (ASPDAC), 2006 (8 nominations out of 424 submissions)

Korean Information and Communication Technology Scholarship for outstanding academic performance in science/engineering, Korea Ministry of Information and Communication, 2002 (46 students selected nationwide in Korea)

New Technology Award for advanced technology and performance in video conferencing software, Korea Ministry of Commerce, Industry and Energy, 2001

Selected Research Contributions

Manufacturability Aware Physical Synthesis: Seminal works on DFM were done where three major manufacturability issues were addressed during physical synthesis in novel manners, namely CMP, random defects, and lithography/printability. These are key works which constitute to synergistic DFM flow [see C12, C5, C6, C8, C10, J2, J4, B1].

Reliability Aware VLSI Physical Synthesis: Novel techniques for reliable VLSI physical synthesis against temperature variation and substrate noise were researched. The first work on temperature aware clock synthesis to minimize thermally induced clock skew was proposed. A high fidelity yet fast graph theoretical substrate noise model was developed and applied to guide an ultra fast substrate noise aware floorplanning for mixed-signal SOCs, which received **Best Paper Nomination in ASPDAC'06** [see C1, C2, J3].

High Performance Global Routing: A new global routing algorithm, BoxRouter pushed the state-of-the-art significantly, and sparked many following research works opening the global routing research renaissance (more than eight follow-up papers within one year after C4). BoxRouter received **Best Paper Nomination in DAC'06**, **ACM/SIGDA Awards in ISPD'07**, **IEEE/CEDA Award**, and helped me receive **SRC Inventor Recognition Award** [see C4, C7, J1, J5, P1, S1, S2].

Parallel Physical Synthesis on Many/Multi-Core Architecture: The first work on parallel physical synthesis methodology to cope with the recent advancements in multi/many-core computing platforms was researched, mainly focusing on physical partitioning, a key to successful CAD parallelization [see C11, P2].

Digital Microfluidic Biochip Chip Design Automation: An efficient digital microfluidic biochip synthesis algorithm was researched to improve the completion of droplet routing. The proposed approach significantly outperformed the start-of-the-art [see C9, J6].

Scan Optimization in VLSI Testing: First temperature aware scan chain optimization to minimize the peak temperature of circuit-under-test (CUT) was proposed. This was also the first work to show that low power testing does not necessarily constitute lower peak temperature due to heat dissipation [see C3].

Teaching Experience

Guest lecturer in a graduate level course, EE 382V: Optimization Issues in VLSI CAD, University of Texas at Austin, Fall 2007.

Guest lecturer in a graduate level course, EE 382V: VLSI Physical Design Automation, University of Texas at Austin, Fall 2006.

Teaching assistant for a graduate level course, EE 382V: System-On-a-Chip Design, University of Texas at Austin, Spring and Fall 2005.

Book/Book Chapters

B1. **Minsik Cho**, Joydeep Mitra, and David Z. Pan, "Manufacturability Aware Routing," *in The Handbook of Algorithms for VLSI Physical Design Automation, CRC Press (Invited)* (edited by Dr. Charles J. Alpert, Prof. Dinesh P. Mehta, and Prof. Sachin S. Sapatnekar)

Journal Articles

J6. **Minsik Cho** and David Z. Pan, "A High-Performance Droplet Routing Algorithm for Digital Microfluidic Biochips," submitted to *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*

J5. **Minsik Cho**, Katrina Lu, Kun Yuan, and David Z. Pan, "BoxRouter 2.0: A Hybrid and Robust Global Router with Layer Assignment for Routability," submitted to *ACM Transactions on Design Automation of Electronic Systems (TODAES)*

J4. David Z. Pan, Peng You, **Minsik Cho**, Anand Ramalingam, Kiwoon Kim, Anand Rajaram, and Sean X. Shi, "Nanometer IC Design and Process Integration: A Survey," under minor revision for *The Journal of Process Control (JPC)* **(Invited)**

J3. **Minsik Cho** and David Z. Pan, "Fast Substrate Noise-Aware Floorplanning with Preference Directed Graph for Mixed-Signal SOCs," accepted to *IEEE Transaction on Very Large Scale Integration Systems (TVLSI)*

J2. **Minsik Cho**, Hua Xiang, Ruchir Puri, and David Z. Pan, "TROY: Track Routing and Optimization for Yield," accepted to *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*

J1. **Minsik Cho** and David Z. Pan, "BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP," *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 26, No. 12, Dec 2007*

Conference Papers

C12. **Minsik Cho**, Kun Yuan, Yongchan Ban and David Z. Pan, "[exact title is not shown for blind review] A paper on lithography aware routing," submitted to *Proc. ACM/IEEE Design Automation Conference (DAC)*, 2008

C11. **Minsik Cho**, James D. Ma, Anthony D. Drumm, Louise H. Trevillyan, Hua Xiang, and Ruchir Puri, "[exact title is not shown for blind review] A paper on parallel design closure," submitted to *Proc. ACM/IEEE Design Automation Conference (DAC)*, 2008

C10. Tung-Chieh Chen, **Minsik Cho**, David Z. Pan, and Yao-Wen Chang, "Metal-Density Driven Placement for CMP Variation and Routability," to appear in *Proc. ACM International Symposium on Physical Design (ISPD)*, Apr 2008

C9. **Minsik Cho** and David Z. Pan, "A High Performance Droplet Router for Digital Microfluidic Biochips," to appear in *Proc. ACM International Symposium on Physical Design (ISPD)*, Apr 2008

C8. David Z. Pan and **Minsik Cho**, "Synergistic Physical Synthesis for Manufacturability and Variability in 45nm Designs and Beyond," to appear in *Proc. ACM/IEEE Asian and South Pacific Design Automation Conference (ASPDAC)*, Jan 2008 **(Invited)**

C7. **Minsik Cho**, Katrina Lu, Kun Yuan and David Z. Pan, "BoxRouter 2.0: Architecture and Implementation of a Hybrid and Robust Global Router," *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov 2007 **(ACM/SIGDA Awards in ISPD'07 Routing Contest, IEEE/CEDA Award, EE Times Coverage)**

C6. **Minsik Cho**, Hua Xiang, Ruchir Puri and David Z. Pan, "TROY: Track Router with Yield-driven Wire Planning," *Proc. ACM/IEEE Design Automation Conference (DAC)*, June 2007

C5. **Minsik Cho**, Hua Xiang, Ruchir Puri and David Z. Pan, "Wire Density Driven Global Routing for CMP Variation and Timing," *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov 2006

C4. **Minsik Cho** and David Z. Pan, "BoxRouter: A New Global Router Based on Box Expansion and Progressive ILP," *Proc. ACM/IEEE Design Automation Conference (DAC)*, July 2006 **(Nominated for Best Paper Award)**

C3. **Minsik Cho** and David Z. Pan, "PEAKASO: Peak-Temperature Aware Scan-vector Optimization," *IEEE VLSI Test Symposium (VTS)*, April 2006

C2. **Minsik Cho**, Hongjoong Shin, and David Z. Pan, "Fast Substrate Noise-Aware Floorplanning with Preference Directed Graph for Mixed-Signal SOCs," *Proc. ACM/IEEE Asian and South Pacific Design Automation Conference (ASPDAC)*, Jan 2006 **(Nominated for Best Paper Award)**

C1. **Minsik Cho**, Suhail Ahmed, and David Z. Pan, "TACO: Temperature Aware Clock Optimization," *Proc. IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, Nov 2005 **(EE Times Coverage)**

US Patents

P2. James D. Ma, **Minsik Cho**, Anthony D. Drumm, Louise H. Trevillyan, Michael W. Dotson, Hua Xiang, Ruchir Puri, "A Method of Partitioning Refinement for Timing Optimization in Computer-Aided Design of Electronic Circuits and Systems," *IBM Disclosure #YOR820070869*, (US Patent Pending)

P1. **Minsik Cho** and David Z. Pan, "Method and Apparatus for Global Routing of an Integrated Circuit," *UT Austin Disclosure #5227*, (US Patent Pending)

Software Packages

S2. **BoxRouter 2.0**, Minsik Cho, Kun Yuan, Katrina Lu, and David Z. Pan
Available at `http://www.cerc.utexas.edu/utda/download/BoxRouter.htm`.

S1. **BoxRouter 1.0**, Minsik Cho and David Z. Pan
Available at `http://www.cerc.utexas.edu/~thyeros/boxrouter/boxrouter.htm`.

Selected Review Activities

- IEEE Transactions on Computer-Aided Design (TCAD)
- IEEE Transactions on Very Large Scale Integration (TVLSI)
- ACM Transactions on Design Automation of Electronic Systems (TODAES)
- IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)
- ACM/IEEE Design Automation Conference (DAC)
- IEEE/ACM International Conference on Computer-Aided Design (ICCAD)
- ACM/IEEE Asian and Pacific Design Automation Conference (ASPDAC)
- IEEE/ACM Design, Automation and Test in Europe (DATE)
- ACM International Symposium on Physical Design (ISPD)

References (In alphabetical order)

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